HOLLISTIC APPROACHES TO DESIGN HIGH SPEED ELECTRONIC CIRCUITS

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The most valuable asset we are given is time. This is perhaps the main motivation behind the desire of human being to minimize the time that it takes for a certain task to be completed. Starting from the middle of 20^{th} century, electronic components brought the hope to perform certain tasks faster than human brain or other existing techniques. Today, we live in an era that billions of computations are performed in less than a second and enormous amount of data can be transmitted between people, thanks to the electronic circuits.

Operation frequency and computation time are the measures of speed in modern electronics. Therefore, we like to find new approaches to push the limits of operation with respect to these metrics. In this thesis, we introduce new design approaches of high speed electronic circuits. The systematic design theory in each chapter is verified by measurement results and compared with simulations. Chapter 1 overviews the advances in each domain and highlights the design challenges ahead of speed enhancement.

In chapters 2 and 3, a new harmonic power maximization theory is proposed which leads to the design of high power active frequency multipliers with record performance. It is shown that by characterizing the nonlinear behavior of a transistor or any nonlinear element, circuit embedding can be selected to max-

imize the power at any desired harmonic. By exploiting this nonlinear model, the design of millimeter wave and sub-millimeter wave circuits becomes more power efficient and higher operation frequencies can be reached compared to linear design approaches.

In Chapter 4, it is shown how emerging technologies such as spin-based devices can outperform the existing technologies in terms of computation time. Essentially, a systematic design of pattern recognition circuits using spin-based devices is provided which is scalable and area efficient. It is shown that by combining circuit design techniques with applied physics principles, these emerging devices improve the existing technology in terms of operation speed, area, and computation burden.

Chapter 5 and 6 highlight two collaboration projects of the author which demonstrate the first terahertz phase-locked transmitter and the first integrated negative inductance circuits. The implementation of these systems bridge the gap between other research areas such as optics and the integrated circuit technology. The findings of the thesis are concluded in Chapter 7.

BIOGRAPHICAL SKETCH

Hamidreza Aghasi was born in Isfahan, Iran 1989. He received the B.Sc. degree in electrical engineering (communication systems) from Sharif University of Technology, Tehran,Iran, in 2011. His undergraduate thesis title was "Source localization based on signal attenuation and delay estimation in sensor networks." He joined the Ultra high-speed Nonlinear Integrated Circuit Lab, Cornell University, Ithaca, NY, USA, in 2011. In 2014, he joined Samsung Research America, Mountain View, CA, USA, and the Display Lab, San Jose, CA, USA, as an Intern.

He is currently a Visiting Scholar with the University of Michigan, Ann Arbor, MI, USA. His current research interests include signal processing, spin-based devices, terahertz power generation, and RF and millimeter-wave design. Mr. Aghasi was a recipient of the Cornell Fellowship in 2011 and the Jacobs Fellowship in 2012. He was also a recipient of the Cornell ECE Innovation Award for the "Teratooth" system in 2013.

To my family for their endless and selfless support and love.

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I am also grateful to Prof. Alyssa Apsel and Prof. Kevin Tang for being in my committee and giving feedback on my research and teaching accomplishments. I would also like to thank Prof. Farhan Rana from Cornell University,

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I have incredible friends. I know Farhad Shirani from age of 5 and within last 23 years, he has consistently been a great friend for me. Navid Naderializadeh and Mohsen Heidari are great examples of caring and supportive friends who happen to be genius intellectuals. Within last ten years of friendship and brotherhood with them, I have never felt alone in the darkest nights of my life. Mohammad Hassan Lotfi, Morteza Hashemi, Shervin Minaee, and Ali Ebrahimi have also been very helpful to me throughout the school years.

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Last but not least, I would love to thank my family members. Without my lovely family who always pumped love and support into my veins, I would have not been able to make one step forward. It will be even scary to imagine how different my life could have been without these heavenly creatures. I am always grateful to my parents who are still inspiring me and leading me towards the right path. Words cannot describe how much I respect my father for being a true scientist and a great role model. He remains as the only role model in my life who instilled the meaning of stamina and patience in my mind. He remains as the most respected scientist for me and the only example of the kind of father that I would like to be. My mother, a gifted heavenly angel with true love and support, has taught me humanity lessons more than any one else and remains a genuine source of love to me. I am very certain that if I dedicate the rest of my life to her, I would not be able to respond her genuine and selfless love. My Brother, Alireza knows very well that he is the most influential individual in my life. After many years, he is still the most caring friend that I could ever wish for. From my very early ages, I have tried to follow the trace of his steps and I cannot be even close to what he is. My lovely sister, Hengaame, means the whole world to me. I cannot even imagine how different my life would have been without her selfless love.

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CHAPTER 1

CHALLENGES IN HIGH SPEED CIRCUIT DESIGN

1.1 High Frequency Operation Limits

Emerging applications of the THz range (0.3-3 THz) include different areas of interest, e.g., molecular spectroscopy, high resolution imaging and ultra-fast communication. To demonstrate THz transmitters, at least milliwatt level of power should be generated in order to battle the high propagation loss in this frequency range.

The reliable implementation of terahertz systems on silicon chips provides a low-cost and scalable solution to the desired applications. The device scaling within the last decade, has provided a mainstream path for circuit designers to design standard circuit topologies at higher operational frequencies. However, as predicted by Moore's law [6], the scaling growth is reaching the limits and a more thorough design approach is required. Besides, the faster devices due to the scaled size, normally come along with a lower breakdown voltage, which limits the power handling capability of the transistor.

In addition, there are specific high frequency design challenges that have to be addressed. First and most importantly, at high frequencies where the operation frequency f_0 is close to the f_{max} of the transistor, the active device exhibits a low power gain. Moreover, the skin effect and substrate coupling deteriorates the power efficiency. These factors are the main obstacles of high power signal generation at the THz range. Fig. 1.1 shows the state-of-the-art terahertz electronic sources.

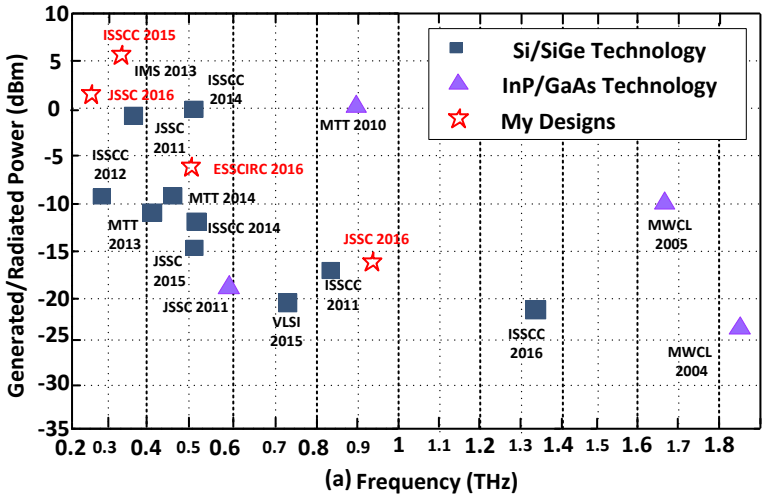


Figure 1.1: the state-of-the-art terahertz and sub-terahertz integrated electronic sources.

Secondly, by increasing the operation frequency beyond f_{max}, the power has to be extracted from the harmonic components of the fundamental signal. Since the harmonic power generation is determined by the nonlinear profile of the device, an accurate nonlinear model to maximize the output power is required. It is noteworthy that the extraction of signal from the harmoinc components, further lowers the power efficiency. This harmonic power modeling and extraction is the most fundamental distinction of THz design with lower frequency circuit design.

Thirdly, the operation bandwidth of THz sources are usually low. In the particular case of harmonic/fundamental oscillators, the insufficient variation of tuning components such as varactors, limits the signal bandwidth. This is why frequency multipliers are a good choice for power generation, where conventional matching techniques can cover the large operation bandwidth.

Lastly, the power distribution/combination of single blocks can add to the

loss of the network. This is particularly important in the traditional design technique where multiple sources are combined to increase the output power level. In order to defeat this factor, novel low-loss microwave structures such as baluns [7] and scalable blocks [8] are required.

Due to all these issues, the generated power levels in Fig.1 for the state-of-the-art THz sources, have been increasing slowly within the last decade. Moreover, it is clear from Fig.1(a) that the generated output power drops with a $1/f^3$ to $1/f^4$ trend by increasing the frequency. Therefore, it still remains a challenge to generate a high power at the terahertz range.

1.2 Challenges of high speed computation

Along with the Moore's prediction, Dennard scaling had brought the hope to increase the clock frequency by reducing the transistor dimensions. However, the underestimated quantum mechanical effects and in particular the "leakage current" started to flaunt their contribution since 2006. In addition it turned out that by shrinking the transistor size, short channel effects such as drain induced barrier lowering and mobility degradation occur. Therefore, fundamental limits for Moore's law were identified and minimum effective gate length of few nanometers is found for the transistors.

In the " integrated digital" domain the clock frequencies have not changed within last few years and emerging technologies such as "spin-based logic" gates with a lower switching energy have been introduced. In addition, "non-Boolean computation", "approximate computation" and "machine learning"

techniques are introduced to overcome the limits of "Boolean computation" for recognition applications. Spintronic devices exhibit unique features such as high density, non-volatility, low switching energy and instant wake up. However, according to Fig.1.2 the energy-delay product of spin-based logic gates is larger than CMOS and implementation of "Boolean logic gates" is not a good benchmark for these devices.

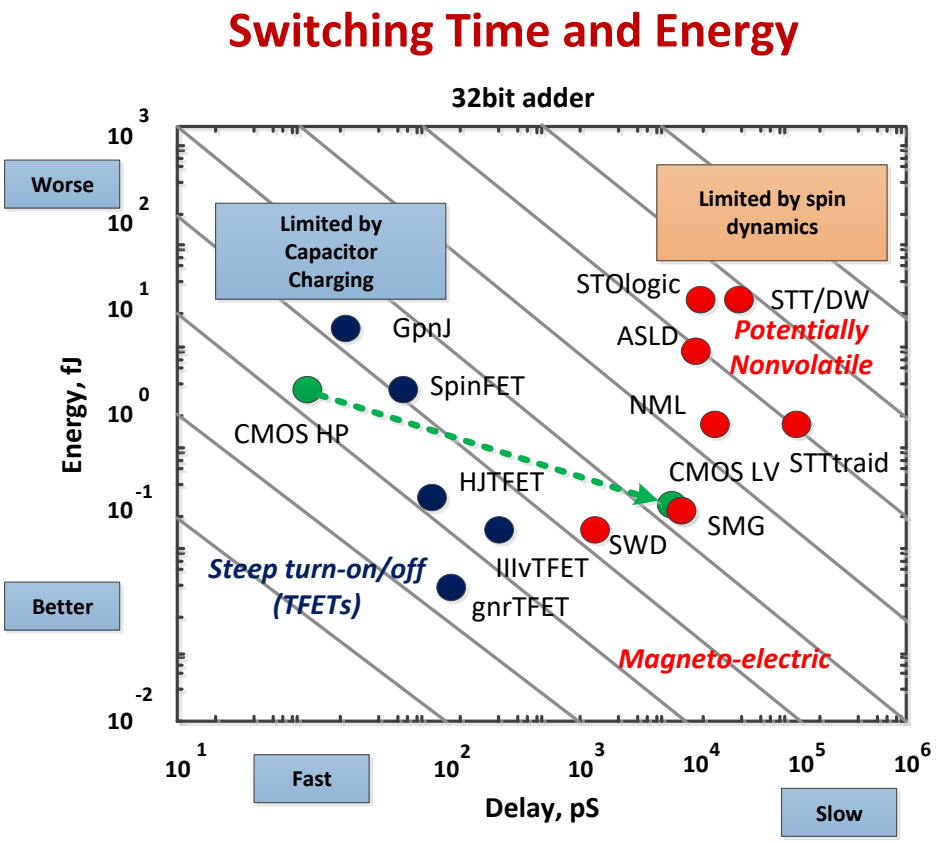


Figure 1.2: Energy consumption and delay of different technologies in implementation of a 32bit adder

CHAPTER 2

A 0.92 THZ SIGE POWER RADIATOR BASED ON A NONLINEAR HARMONIC GENERATION THEORY

2.1 Introduction

A growing interest in sub-mm wave (0.3 to 3 THz) circuits and systems has been witnessed within the last decade. This is mainly due to the plethora of opportunities within this previously unexplored electromagnetic spectrum [9]-[12]. The characteristic of absorption profiles and proliferation of molecular resonances makes this region of spectrum a unique platform of material spectroscopy. Higher spatial resolution compared to lower frequency ranges and the non-ionizing nature compared to the higher frequency radiations (e.g., the X ray) adds to the exclusive features of the THz frequency window for imaging applications [12]-[14].

At the early stages of investigation, compound semiconductors [15]-[23], gifted with a high speed operation potential (f_{max} >300 GHz) and quantum cascade lasers [24], brought the hope of THz power generation. However, they did manifest challenges such as stringent operation requirements (e.g., the low temperature) and high cost. CMOS circuits, were investigated as the next platform, due to their lower cost and integration capability. The first CMOS mm-wave circuits were high bandwidth transceivers and imaging/sensing circuits [25]-[41].

After the successful demonstration of CMOS mm-wave circuits, fundamental and harmonic oscillators [42]-[54] were designed to reach a higher operation frequency.Due to the insufficient DC-to-RF efficiency and the limited bandwidth

of the oscillators, frequency multipliers were explored to boost the performance [55]-[63]. Despite the high output power of passive and active CMOS frequency multipliers, frequency tuning [59], phase-locked operation [60], and closer to f_{max} operation [61], [62], were the pending milestones before a sub-mm wave transceiver could be demonstrated.

In a parallel route, the feasibility of on chip antenna demonstration opened the path for THz radiators [58], [64] and detectors [65]-[68]. The novel radiation techniques introduced in some of these works [65]-[69] was later used in phased-arrays [70].

At the THz range where CMOS has limited capabilities, the BiCMOS technologies joined the relay and ignited the path towards higher power generation [**?**], [69]. The higher break down voltage, higher operational frequency (f_{max} >300 GHz) and the more nonlinear I-V characteristic were the assets that CMOS lacked. Taking advantage of these unique features, 3.3 mW of power was achieved at 320 GHz in a (f_T/f_{max}=220/280 GHz) process. Similarly, in [69], 1 mW of power was generated at 0.53 THz inside a re-configurable array.

In all the mentioned beyond f_{max} demonstrations the power extraction is through the harmonics of the fundamental frequency. Previous work on maximizing the fundamental power [62], [58] could enhance the harmonic power significantly due to operation in a more nonlinear region. However, the power generation at higher harmonics still requires a thorough modeling of the harmonic signal. A systematic design methodology to generate maximum harmonic power based on a nonlinear model remains as the missing piece before circuit designers could demolish the obstacle of beyond 1 THz operation using the existing transistor technologies.

In order to push the operation limits of electronic circuits, a systematic design approach is required. The proposed design methodology should provide an accurate model of the nonlinear device. Moreover, the effect of circuit topology and the embedding network on the harmonic power should be characterized. This is the main intention behind the proposed design approach in this paper. We introduce a nonlinear characteristic of the active device based on the Volterra theory [72], which can be exploited to model any arbitrary nonlinear component. Based on the proposed model, the optimum embedding network and the nonlinearity enhancement techniques are proposed which yield to a high harmonic power.

Using a 130nm SiGe:C BiCMOS process (f_T/f_{max}=220/280 GHz, V_{ceo}=1.6V [71]), a frequency quadrupler radiator at 0.92-0.944 THz is designed. The circuit achieves a generated output power of -17.3 dBm at .928 THz, which results in -10 dBm of EIRP and stands among one of the highest frequency radiators in Si/SiGe processes. The nonlinear model of the active device is presented in Section II. The harmonic power optimization is presented in Section III. Section IV covers the design of a high power frequency quadrupler. The measurement results and comparison with the state-of-the-art are presented in Section V and the paper is concluded in Section VI.

2.2 Nonlinear Model of the two-port device

An accurate model of transistor or any nonlinear component is essential to determine the mechanisms of harmonic signal generation. The proposed model should easily cope with arbitrary embedding networks and also encapsulate

the variations of device behavior, e.g., the frequency dependence of the nonlinear profile. In this section, we propose a model based on the Volterra-Weiner theory [72], which meets the desired criteria.

2.2.1 Review of Volterra-Weiner Theory of Nonlinear Devices

In 1958, Weiner re-arranged the nonlinear series that Volterra had found in 1887 and that is why engineers mostly refer to Volterra-Weiner theory [72]. These series capture different linear and nonlinear effects that contribute to output components. Both time domain and frequency domain representations of these series exist; however, we are interested in frequency domain equations as we would like to capture the dynamics of harmonic variations. Utilizing the multi-dimensional Fourier transform, the frequency correspondence of each kernel [72] k_i is defined as,

$$K_i(j\omega_1, \cdots j\omega_i) = \int_{\mathbb{R}} \cdots \int_{\mathbb{R}} k_i(\tau_1 \cdots \tau_i) e^{-j(\omega_1\tau_1 + \cdots \omega_i\tau_i)} d\tau_1 \cdots d\tau_i. \tag{2.1}$$

As an example, for $i = 1$, the Fourier transform of linear system $K_1(j\omega)$ is obtained, i.e.,

$$Y_1(j\omega) = K_1(j\omega)X(j\omega). \tag{2.2}$$

Similarly, for a P^{th}-order operator, utilizing the P-dimensional Fourier transform,

$$Y_P(j\omega_1 + \cdots + j\omega_P) = K_P(j\omega_1, \cdots, j\omega_P)X(j\omega_1) \cdots X(j\omega_P). \tag{2.3}$$

The equation in (2.3) is the general form of an intermodulation. As an example, for a 2^{nd}-order input signal, containing ω_0 and $2\omega_0$ components, $K_2(j\omega_0, j2\omega_0)$ represents the fundamental and second harmonic intermodulation to generate the 3^{rd} harmoinc component of the output. For identical ω_i's, K_P represents the P^{th}-order nonlinear transfer of ω_i at the input to $P\omega_i$ at the output. For $P = 1$, (2.3) is a linear operator.

We are mostly interested in the response of the system to a periodic time domain signal, e.g.,

$$x(t) = \sum_{i \leq L} c_i.cos(i\omega_0 t), \tag{2.4}$$

which is a real periodic signal that contains the harmonics up to the L^{th}-order. For this input, the output time domain signal $y(t)$, is the combination of linear, nonlinear and intermodulation operators. For example, the response of a second order system to the input $Acos(\omega_0 t)$ is,

$$y(t) = 2(\frac{A}{2})^2 Re\{K_2(j\omega_0, j\omega_0)e^{j2\omega_0 t}\} + ARe\{K_1(j\omega_0)e^{j\omega_0 t}\} + 2(\frac{A}{2})^2 Re\{K_2(j\omega_0, -j\omega_0)\}, \tag{2.5}$$

where the first term represents the 2^{nd} order operator from ω_0 to $2\omega_0$, the second term is the linear response of the system at ω_0 and the last term is the intermodulation. Without showing the complex general expression for the case of multi-harmonic input signal applied to a higher order nonlinear system [72], we will introduce a two-port nonlinear model, in the next subsection.

2.2.2 Nonlinear Two-port Device Modeling

To propose a general nonlinear model, we should capture the important nonlinear mechanisms in different types of transistors, e.g., MOS and BJT. The standard simplified circuit model of these devices are shown in Fig. 2.1. According to these models, the three-port device can be modeled with two ports if the voltage variatinos at the third port (the emitter in BJT or source in MOS) are negligible. The linear two-port model of transistors is shown in Fig. 2.2(a). Based

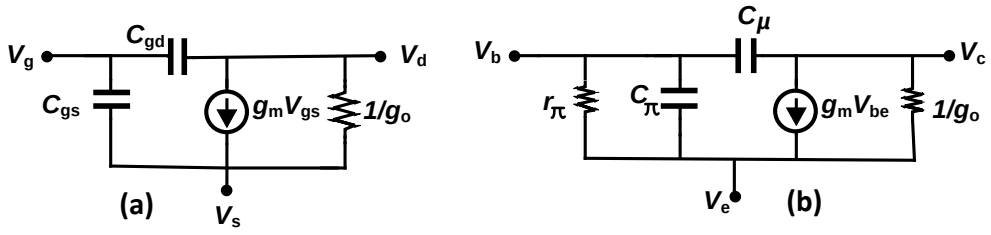


Figure 2.1: (a) Simplified circuit model of (a) MOS transistor and (b) BJT transistor.

on what Mason introduced in [73], activity condition of this three-terminal (two-port) device is defined by an invariant function U. In this terminology, the three-terminal device is embedded in a 4-port, linear, lossless, reciprocal network, as shown in Fig. 2.2(c). Based on the method proposed in [62], the net power flowing out of the device determines the device activity. Moreover, optimum conditions to generate maximum power at the oscillation frequency are calculated in [62]. The elements of the admittance (Y) matrix, determine the values of these optimum conditions.

The linear two-port model fails to address the harmonic generation due to the device nonlinearity. Therefore, we would like to find a two-port model

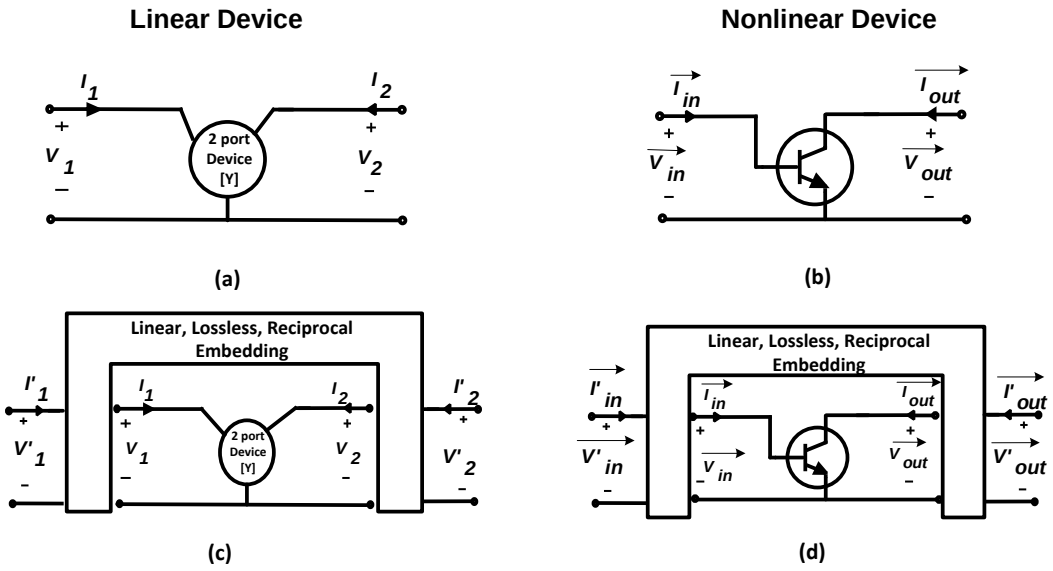


Figure 2.2: (a) A three-terminal linear two-port device, (b) three-terminal nonlinear two-port device, (c) a linear device embedded in a 4-port network and (d) a nonlinear device embedded in a 4-port network.

which can capture the major nonlinear mechanisms in the transistor. By selecting invariant DC conditions across the transistor, the variations in the device capacitors can be almost negligible [74]. However, for a fixed DC condition, the transistor still exhibits nonlinear performance due to the current distortion of the output channel. The output channel distortion is mainly due to the transconductnace g_m and the output conductance g_o. For the two-port model in this work, we would consider a nonlinear profile for any element of Y matrix which contains g_m or g_o and leave the rest simply as linear parameters. The reader can verify that Y_{21} and Y_{22} of the active devices in Fig. 2.1 contain terms from g_m and g_o, while Y_{11} and Y_{12} do not.

Therefore, similar to the terminology of [73], in this paper, the transistor is modeled as a two-port network, as shown in Fig. 2.2(b). Consequently, the tran-

sistor can be embedded in a linear, reciprocal network as shown in Fig. 2.2(d). The multi-harmonic arrays of voltage and current $\overrightarrow{I}$ and $\overrightarrow{V}$ are considered in this model to mention the fact that current and voltage components at at any harmonic is dependent on components from other harmonics.

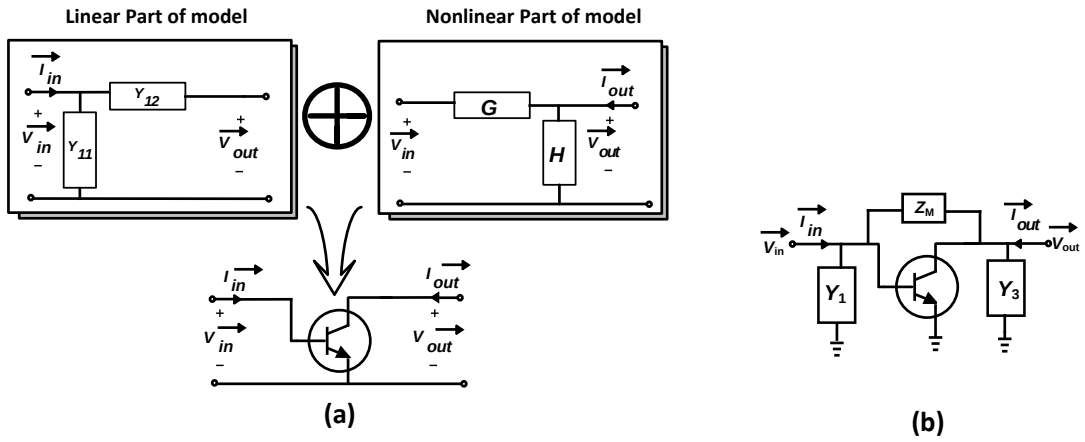


Figure 2.3: (a) Nonlinear two-port representation of device and (b) embedded with a general passive network.

The current generation mechanisms in transistors dictate a nonlinear relationship between the output current $\overrightarrow{I_{out}}$ and input/output voltages ($\overrightarrow{V_{in}}$ and $\overrightarrow{V_{out}}$). However, the input admittance (Y_{11}) and the feedback admittance (Y_{12}) of the transistor, are still considered as linear functions. In the proposed model of Fig. 2.2(a), the G and H functions, represent the different order transconductance functions of $\overrightarrow{V_{in}}$ to $\overrightarrow{I_{out}}$ and conductances of $\overrightarrow{V_{out}}$ to $\overrightarrow{I_{out}}$, respectively. The coefficient G_{ij} is defined as the gain from the i^{th} harmonic of the input voltage to the j^{th} harmonic of the output current. Similarly, H_{ij} is defined as the gain from the i^{th} harmonic of the output voltage to the j^{th} harmonic of the output current. It is easily induced that for identical i and j, the operator is linear and for different i and j it is a nonlinear or intermodulation operator. If j is a multiple of i,

the G_{ij} and H_{ij} coefficient represent a j/i-order nonlinear operator, i.e.,

$$G_{ij}(i\omega_0, j\omega_0) = \frac{\Delta I_{out,j\omega_0}}{\Delta V_{in,i\omega_0}^{j/i}}, \tag{2.6}$$

$$H_{ij}(i\omega_0, j\omega_0) = \frac{\Delta I_{out,j\omega_0}}{\Delta V_{out,i\omega_0}^{j/i}}. \tag{2.7}$$

It is noteworthy that each coefficient is calculated when the other voltage terms are held constant. We have to mention that the proposed model has a major difference with broadband polyharmonic model [75]. The assumption of dominant fundamental signal in [75] is essential to use the harmonic superposition principle [76]. Therefore, the coefficients in [75] are dependent on the amplitude of the fundamental voltage. However, in the proposed model, the voltage variations are captured in the calculation scheme of coeffiicients; hence, the G and H coefficients are assumed amplitude-independent. The values of nonlinear operators are calculated for a fundamental frequency of ω_0 and we simply denote them as G_{ij} and H_{ij} coefficients. In case that j is not a multiple of i, the G and H are intermodulation operators. Based on (2.3), there are many intermodulations between any two harmonics. As an example $H_2(2\omega_0, \omega_0)$, $H_3(2\omega_0, 3\omega_0, -2\omega_0)$, $H_4(2\omega_0, 3\omega_0, -\omega_0, -\omega_0)$, all relate the second harmonic of the output voltage and the 3^{rd} harmonic of the output current in a transistor with 4^{th} order nonlinearity. However, as we simulated, the numerical values of the intermodulation components at higher frequencies are small; hence, we neglect the effect of intermodulation terms. In contrast, for low frequency highly-nonlinear circuits such as mixers, these coefficients should be considered for the analysis of mixing products. In [72], the calculation of these intermodulation coefficients is shown.

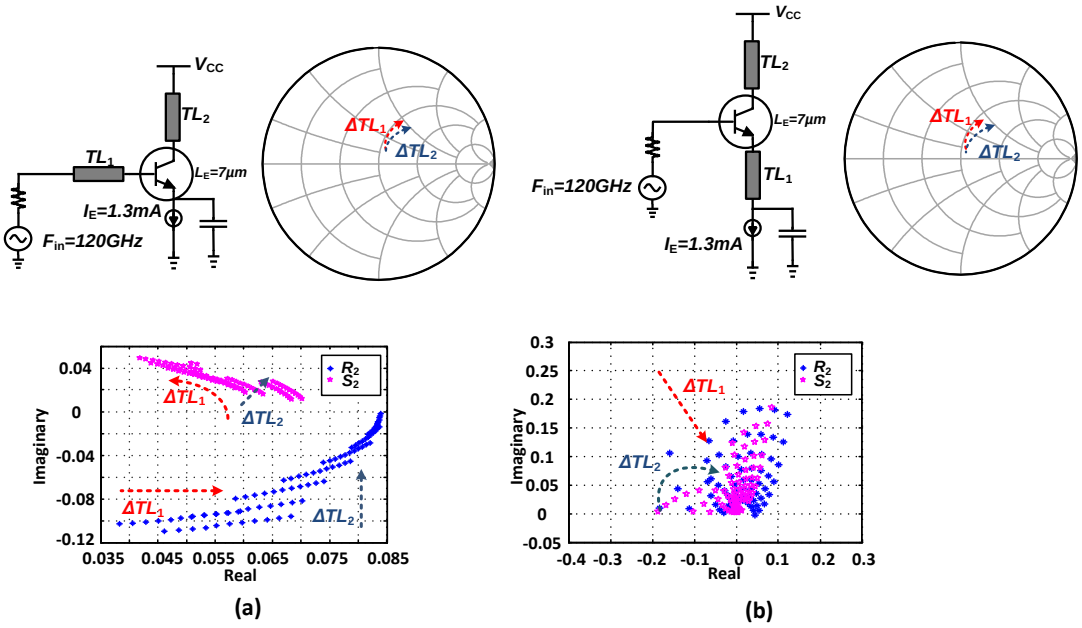


Figure 2.4: (a) the variations of R_2 and S_2 with respect to the illustrated changes of TL_1 and TL_2 and, (b) the similar variations on the transmission line values in a different topology. For an identical transistor, the topology determines the behavior of the ratio functions.

2.2.3 Combination of linear passive network and nonlinear device

As shown in [72], the interconnection of two nonlinear systems, is the sum value of the corresponding kernels in time domain which translates to summation of transfer functions in frequency domain. Based on (2.2), a linear system can be considered as a first-order nonlinear system. Therefore, by placing the transistor in a linear embedding network, the linear operators of the device (Y_{11}, Y_{12}, G_{ii} and H_{ii}) are updated accordingly; however, the nonlinear coefficients remain unchanged. For example, by placing the transistor in the general embedding network of Fig. 2(b), the new linear operators of transistor, are updated accord-

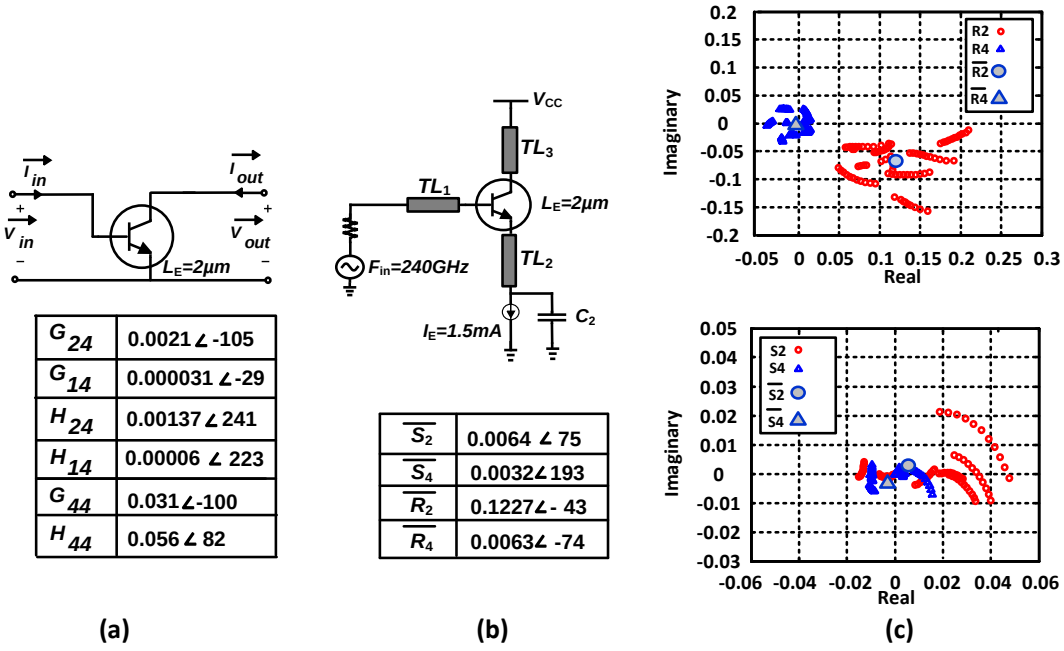


Figure 2.5: (a) The selected transistor size and the corresponding G and H coefficients, (b) topology of the frequency quadrupler and, (c) the variations of the topology R_i and S_i functions by changing TL_1, TL_2 and TL_3. The mean value of the functions and their relative location on the real-imaginary axis are also shown.

ingly, i.e.,

In these equations, $Y_{ij,M}$ are the elements of the Y matrix of Z_M which are calculated to be

The proposed nonlinear model is utilized inside any arbitrary circuit topology. Using this result, the nonlinear harmonic power optimization is performed in the next section.

2.3 Nonlinear Harmonic Power Optimization

When the transistor operates at a fundamental frequency of ω_0, the nonlinear operators generate components at different harmonics, i.e., $n\omega_0$. For a more nonlinear device, the higher order operators appear and contribute to power generation at higher harmonic index. The frequency dependence of the G and H operators, takes into account the variations of device characteristic by frequency. In order to evaluate the device performance at a certain harmonic, the real power flowing out of the device at the particular harmonic is defined as,

$$P_{R,i} = \boldsymbol{Re}\{V^*_{in,i} I_{in,i} + V^*_{out,i} I_{out,i}\} \tag{2.8}$$

The expression in (2.8) consists of two power terms at the input and output ports of the device. This definition is more comprehensive for oscillators, where the total power determines the DC-to-RF efficiency. However, in circuits with input, such as frequency multipliers, the transistor is fed with RF power at ω_0 and the output power, is extracted at a certain harmonic of the fundamental frequency. Therefore, we solely consider the real power at the output port,

$$P_{R,out,i} = \boldsymbol{Re}\{V^*_{out,i} I_{out,i}\}. \tag{2.9}$$

Based on the harmonic index i, particular nonlinear operators that generate $I_{out,i}$ are considered. The general expression of (2.9) is written as,

$$P_{R,out,i} = \boldsymbol{Re}\{V^*_{out,i}[G(\vec{V_{in}}) + H(\vec{V_{out}})]\}, \tag{2.10}$$

where $G(\vec{V_{in}})$ and $H(\vec{V_{out}})$ represent the contribution of input voltage array and

output voltage array on $I_{out,i}$, respectively. As an example, if the harmonic content up to the 4^{th}-order is considered in a nonlinear transistor, operating at the fundamental frequency of ω_0,

$$I_{out,4} = G_{14}V_{in,1}^4 + G_{24}V_{in,2}^2 + G_{44}^N V_{in,4} + H_{14}V_{out,1}^4 + H_{24}V_{out,2}^2 + H_{44}^N V_{out,4}, \qquad (2.11)$$

represents the major terms that generate the harmonic current, $I_{out,4}$. It is noteworthy that the third harmonic and higher harmonics impact the output current at the fourth harmonic, only through intermodulation terms. As mentioned before, based on the discussion on the relative value of these terms compared to those in (2.11), the intermodulation terms are neglected. The expression in (2.11) contains different voltage components and the power optimization is not trivial. Moreover, the N exponent on the linear Volterra coefficients, exhibits the variation of these coefficients by the linear passive network. Therefore, we need to reduce the number of voltage components and simplify the harmonic current expression. Simultaneously, the impact of the selected circuit topology on the nonlinear device should be characterized.

2.3.1 Impact of Circuit Topology and the Ratio Functions

The number of independent parameters in (2.11) can be reduced by relating the harmonic components and fundamental components. However, the ratio of harmonic voltage components and the fundamental components, are determined by the circuit topology. In other words, the structure of passive network, the initial DC conditions and transistor size determine the ratio of the harmonic and the fundamental signals at the input and output ports of the device.

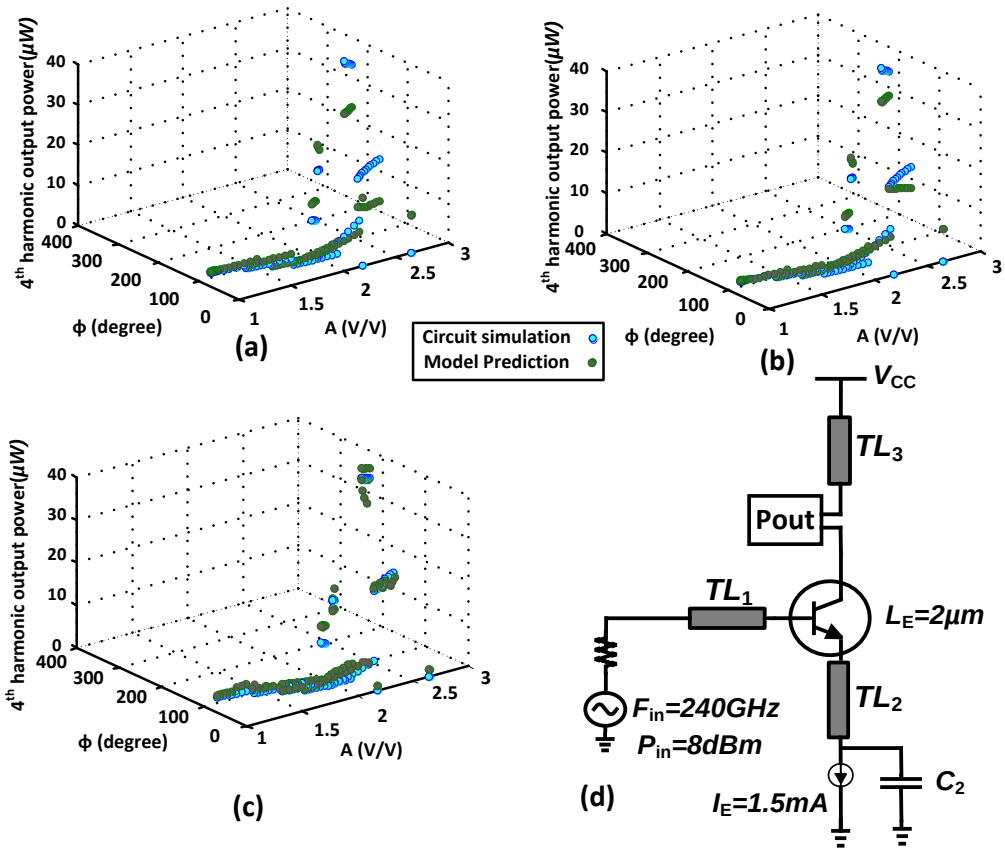


Figure 2.6: (a) the harmonic power prediction using the approximate model (2.21), compared with the circuit simulations, (b) the harmonic power prediction using the moderate model (2.19), compared with the circuit simulations, (c) the harmonic power prediction using the accurate model (2.15) compared with circuit simulations and (d) the circuit schematic used in these simulations.

Accurate Model

For any fixed circuit topology (invariant passive network with variable values, constant bias conditions and invariant transistor), the "ratio functions" are defined, i.e.,

$$V_{in,i} = R_i(V_{in,1}), \tag{2.12}$$

$$V_{out,i} = S_i(V_{out,1}), \tag{2.13}$$

and for the 4^{th} harmonic current,

$$I_{out,4} = G_{14}V_{in,1}^4 + G_{24}R_2^2(V_{in,1}) + G_{44}^N R_4(V_{in,1}) + H_{14}V_{out,1}^4 + H_{24}S_2^2(V_{out,1}) + H_{44}^N S_4(V_{out,1}), \tag{2.14}$$

$$P_{R,out,4} = \boldsymbol{Re}\{S_4^*(V_{out,1}^*)I_{out,4}\}. \tag{2.15}$$

By changing the values of passive components around the transistor in a fixed topology, the values of the ratio functions change. More importantly, as shown in Fig. 2.4, for a certain transistor, the ratio functions behave completely different when the topology is changed. This is why the topology invariance constraint is imposed in this paper to simplify the power optimization.

In Appendix.1, an analytical study of ratio functions are shown for the circuit of Fig. 2.4(a). The amplitude and phase of each harmonic voltage component inside this simple circuit is dependent on many parameters, e.g., the width of transmission lines, the input source impedance and the transistor linear/nonlinear operators. The trend and closed-form expressions can become very complicated in circuits with more passive components. Therefore, we would like to find a simpler way to perform the power optimization. In the next two subsections, we will introduce two simpler approximations, which can be used as an estimation to find the optimum conditions of harmonic power.

Moderate Model

As the values of the passive components change, the ratio values also change slightly for a fixed topology (Fig. 2.3). In addition, the variation of passive components changes G_{ii} and H_{ii}. We prefer an easier power optimization and substitute the ratio functions with a fixed value (e.g., ratio constant) for the selected topology. Without loss of generality, the mean value of the ratio values ($\bar{R}_i$ and $\bar{S}_i$) is selected to be the ratio constant as shown in Fig. 2.5(c), i.e.,

$$R_{i,m} = \bar{R}_i, \tag{2.16}$$

$$S_{i,m} = \bar{S}_i, \tag{2.17}$$

$$I'_{out,4} = G_{14}V^4_{in,1} + G_{24}R^2_{2,m}V^2_{in,1} + G^N_{44}R_{4,m}V_{in,1} + H_{14}V^4_{out,1} + H_{24}S^2_{2,m}V^2_{out,1} + H^N_{44}S_{4,m}V_{out,1}, \tag{2.18}$$

$$P_{R,out,4} \simeq \boldsymbol{Re}\{S^*_{4,m}V^*_{out,1}I'_{out,4}\}. \tag{2.19}$$

Approximate Model

Taking into account the variations of the linear coefficients with the passive components in (2.15) and (2.19) adds to the complexity of the power expression. To achieve a faster power estimation, we sacrifice the accuracy by neglecting this effect. As shown later, this approximate version still guides us through the maximum power location. Therefore, we neglect the impact of passive component variations on the linear coefficients, i.e.,

$$I''_{out,4} = G_{14}V^4_{in,1} + G_{24}R^2_{2,m}V^2_{in,1} + G_{44}R_{4,m}V_{in,1} + H_{14}V^4_{out,1} + H_{24}S^2_{2,m}V^2_{out,1} + H_{44}S_{4,m}V_{out,1}, \tag{2.20}$$

$$P_{R,out,4} \simeq \boldsymbol{Re}\{S^*_{4m}V^*_{out,1}I''_{out,4}\}. \tag{2.21}$$

The final simplified harmonic power expression is obtained by substituting $V_{out,1} = A_1V_{in,1}$, where $A_1 = Ae^{j\phi}$ is a complex gain. This enables us to find the optimum conditions of harmonic power generation in terms of A and ϕ. Therefore, the harmonic power is related to the circuit topology (ratio constants), the transistor nonlinearity (G_{ij} and H_{ij} coefficients) and the fundamental frequency gain, A_1. Moreover, the dependency on the amplitude of $V_{in,1}$ captures the harmonic power variations by changing the input power at the fundamental frequency.

2.4 Design of a High Power Frequency Quadrupler

Based on the developed model in the previous section, we design a high power THz frequency quadrupler. The utilized technology (BiCMOS 130 nm SiGe:C) has a f_{max} of 280 GHz [77]; hence, the input frequency is selected below f_{max} to sustain the high swing of fundamental frequency. For a target output frequency of 0.92-0.96 THz, by extraction of the 4^{th} harmonic, an input frequency of 230-240 GHz is selected.

2.4.1 Transistor Selection

In selection of the transistor, the major consideration is regarding the parasitics and current drive. For THz operation, the transistor size is selected to be small in order to shrink the parasitic resistance and capacitance. On the other hand, the smallest possible width for MOS or emitter length for BJT does not provide sufficient transconductance to generate high output power. This is the main reason that a bipolar transistor (Q_1) with an emitter length of $2\mu m$ is selected as shown in Fig. 2.5(a). The Volterra coefficients of the selected transistor are also listed in Fig. 2.5(a).

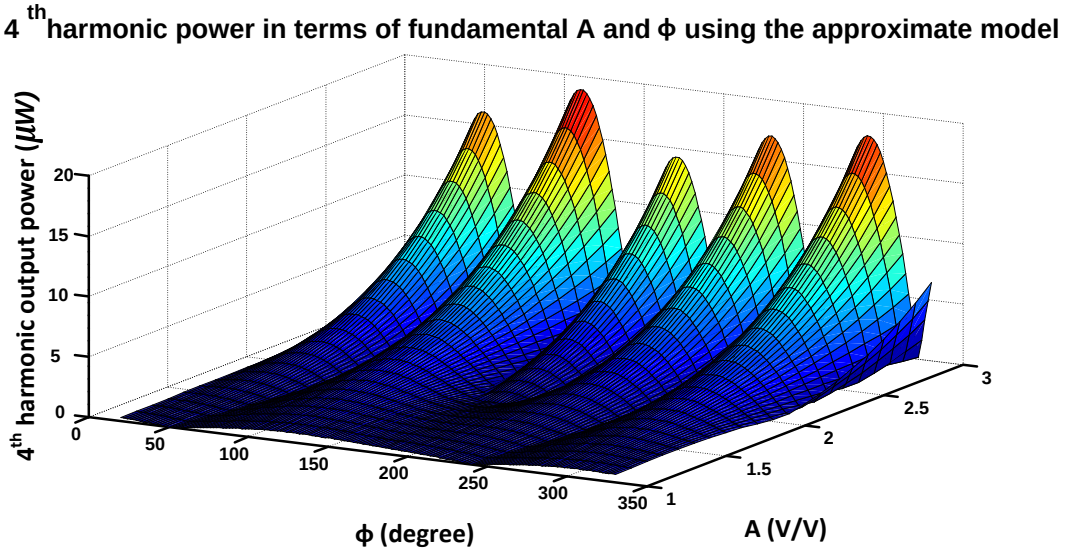


Figure 2.7: According to the approximate model, we can find the location of optimum harmonic conditions in the $[A, \Phi]$ plane. In order to maximize the harmonic power, the transmission lines are selected to reach these optimum conditions.

2.4.2 Circuit Topology and Optimum Embedding Network

Among different circuit configurations for a bipolar transistor, the common-emitter (CE) topology of Fig. 2.5(b) is selected. Due to the extraction of the output current from the collector node, the CE topology conserves the nonlinear profile of the device and generates high power harmonics. The second reason is about the matching feasibility and the power extraction. The base transmission line TL_1 and the junction capacitor of Q_1, are used for the input power matching. On the other hand, adding the TL_1 transmission line at the base determines the value of ratio constants (i.e., R and S) at the input. By adding the TL_2 at the emitter, the values of R_i and S_i constants are changed again. Consequently, the addition of TL_2 transmission line, transforms the impedance seen by the current source and the bypass capacitor (C_2) to a smaller value. For the selected transistor and topology, by changing the characteristic of TL_1, TL_2 and TL_3, the ratio functions and corresponding mean values (ratio constants) are shown in Fig. 2.5(b) and Fig. 2.5(c). The power expressions in (2.15),(2.19) and (2.21) are used to predict the harmonic power for the circuit topology of Fig. 2.5. As the results in Fig. 2.6 illustrate, all the 3 different models, exhibit a close match to the circuit simulations. This is the main reason that the simplified expression in (2.21) is used in Fig. 2.7 to find the location of maximum 4^{th} harmonic power. In order to reach these optimum conditions, transmission lines can be selected similar to [62].

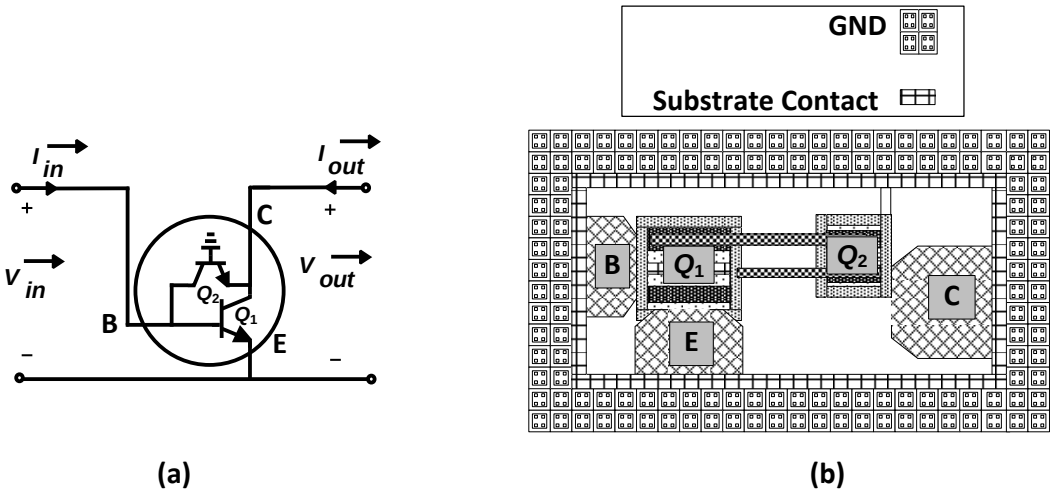


Figure 2.8: (a) the nonlinearity manipulation by adding transistor Q_2 and, (b) the layout of the Q_1 and Q_2 transistor combination.

2.4.3 Device characteristic manipulation

Besides the passive component effects, the nonlinear device can be manipulated to further increase the harmonic power. As shown in Fig. 2(b), by adding a parallel component with the transistor, the linear operators, i.e., G_{ii} and H_{ii} are manipulated. This is particularly important for operation at higher harmonics where multiple harmonics are involved in the power generation and more adjustments are required before reaching the optimum power. Based on the value of the G and H functions and the S and R coefficients of the selected topology in Fig. (4), to achieve a higher 4^{th} harmonic power: 1) The magnitude of G_{44} should be increased and 2) the value of S_2 and R_2 at the output and input ports of device should be preserved. The first condition is satisfied by adding a passive component which exhibits a low impedance (high admittance) at the 4^{th} harmonic frequency. However, the selected component has to provide a high impedance (ideally zero admittance) at the fundamental and second harmonic

frequencies in order to preserve the R_2 and S_2 constants. Therefore, we have to add a small capacitor in parallel with the transistor. Since it is not straightforward to design small capacitors at the THz frequency range, a bipolar transistor in cut-off region is utilized instead. The selected $0.6\mu m$ transistor, exhibits a high impedance at the lower harmonics and low impedance at the fourth harmonic. In order to minimize the parasitics of the combination of the two transistors, the substrate contact of the confined transistors is redrawn inside a compact structure as shown in Fig. 2.8. As shown in Fig. 2.9, by combination of Q_1 and Q_2, the predicted harmonic power at the design point increases by 2.2 dB, compared to the case that Q_2 is not added. In the circuit simulations, a 2dB power increment is achieved.

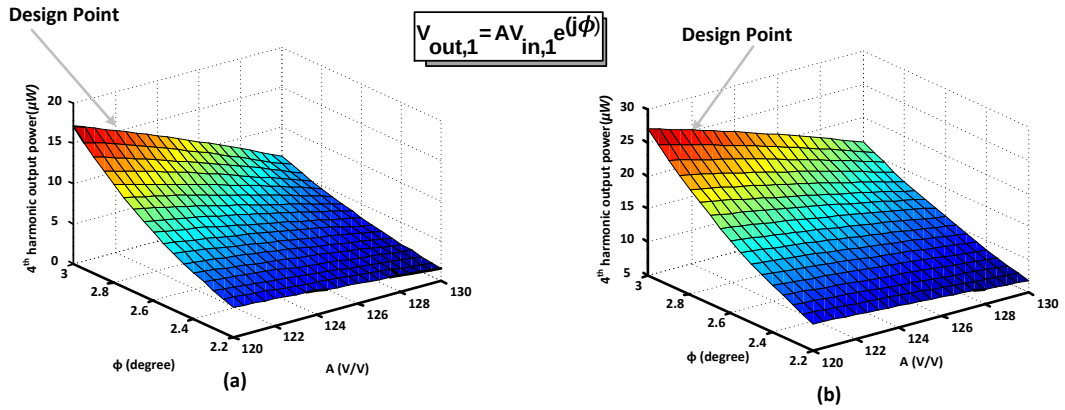


Figure 2.9: (a) The model prediction of the harmonic power in the vicinity of optimum point for the selected topology when (a) Q_1 is the only nonlinear component and (b) the Q_1 and Q_2 combination is the nonlinear component.

In order to design close to the optimum point, it is noticed that no extra passive components are allowed, as the circuit topology changes and the ratio constants have to be updated. However, as it is verified by the circuit simulations in Fig. 2.5, there exists a combination of TL_1, TL_2 and TL_3 which operates

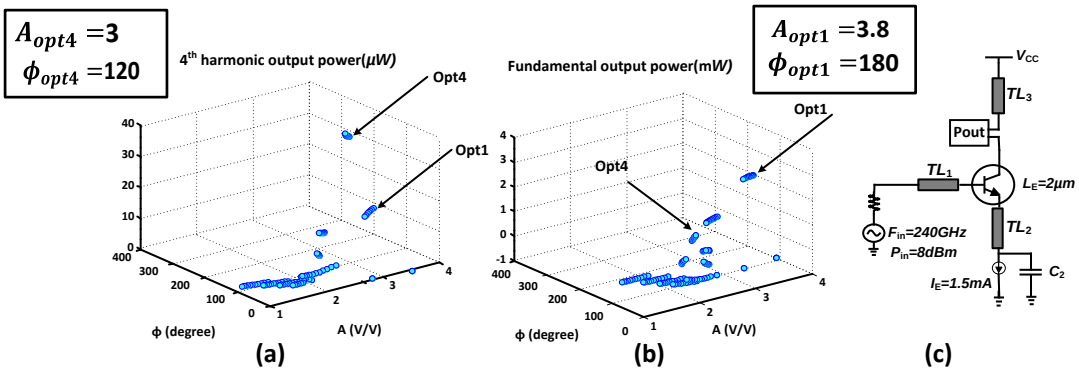


Figure 2.10: (a) the circuit simulations of the fourth harmonic output power and (b) the simulated fundamental power. It is clear that the optimum conditions of the fundamental and fourth harmonic, Opt1 and Opt4, are different, (c) the simulation testbench.

close to the optimum point of Fig. 2.7. This point is indicated as Opt4 in Fig. 2.10. On the other hand, due to the nonlinear profile of transistors, the harmonic power is not maximized by providing the optimum fundamental conditions. This phenomenon is illustrated in Fig. 2.10, where the fundamental and fourth harmonic output power reach maximum at different points. This means that utilizing a linear assumption, fails to guide us towards the optimum point for the harmonic power. And finally, it is noteworthy that based on the proposed theory, the maximum harmonic power is found for a particular topology. This is the main difference of this model with previous linear model techniques. The proposed systematic design flow of THz frequency multipliers is shown in Fig. 2.11.

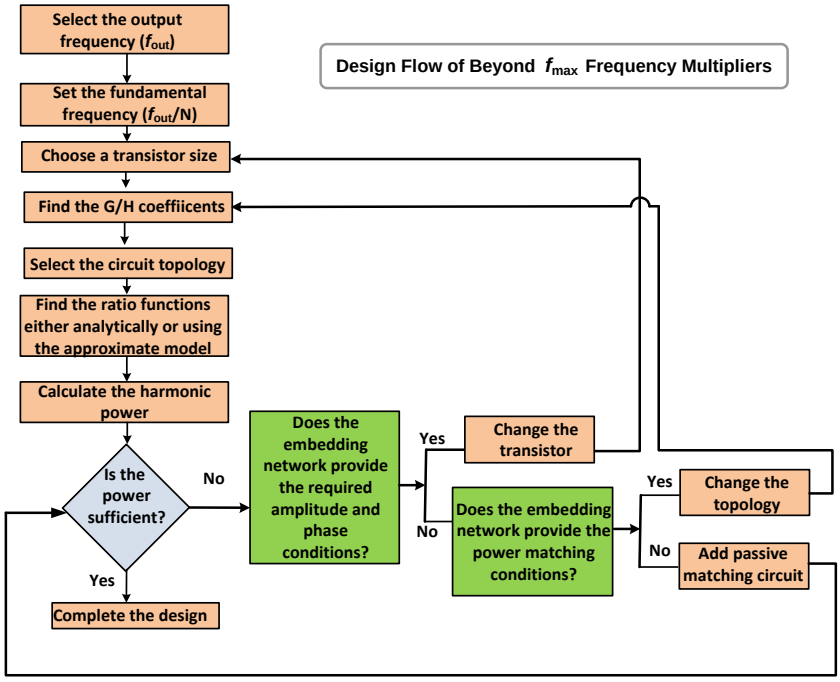


Figure 2.11: The summary of the proposed design flow for THz frequency multipliers

2.4.4 Matching Conditions

The output embedding at the collector side is selected such that a large fundamental voltage swing is achieved for the selected transistor size. It should also provide the matching conditions for the output signal and block the current flow of unwanted harmonic components to the output. For this particular frequency quadrupler, the output network is expected to provide the conjugate matching condition for the 4^{th} harmonic signal. In addition, the harmonic components which are crucial for the power generation at the output frequency are kept confined at the transistor.

As illustrated in Fig. 2.12, by differential operation, the powerful fundamental current does not flow toward the common node and remains inside the

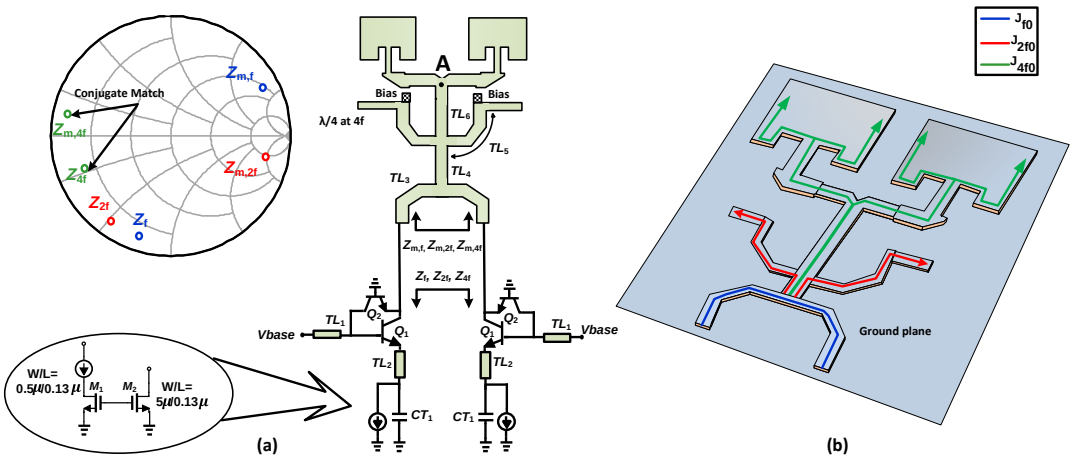


Figure 2.12: (a) frequency quadrupler schematic and the matching conditions at different harmonics, and (b) the distribution of the current intensity of the harmonics.

transistor. However, the second harmonic currents of the two transistors in a differential circuit are in phase and can potentially flow towards the output antenna feed point (node A). To block the flow of second harmonic, a matching network is utilized in the circuit which provides high impedance to the second harmonic current and blocks it before reaching the output node. This condition is provided by adding the stub transmission lines (TL_5). On the other hand, the impedance of the stub is seen high at the fourth harmonic and the corresponding current component has to flow through TL_6 and reach node A.

2.4.5 Single to Differential Power Conversion

Based on the mentioned advantage of differential operation, the input power coming from the external source is converted into differential form, using a balun [78]. There are mainly three considerations on the selected structure of

this balun: 1) It has to be wideband, 2) it should exhibit a low conversion loss and 3) the selected architecture should embed in the layout pattern imposed by the rest of the circuit. Therefore, a microwave passive short-open balun [79] is designed as shown in Fig. 2.13. The selected balun has a low conversion loss (< 0.8 dB) and preserves the phase/amplitude match at the input.

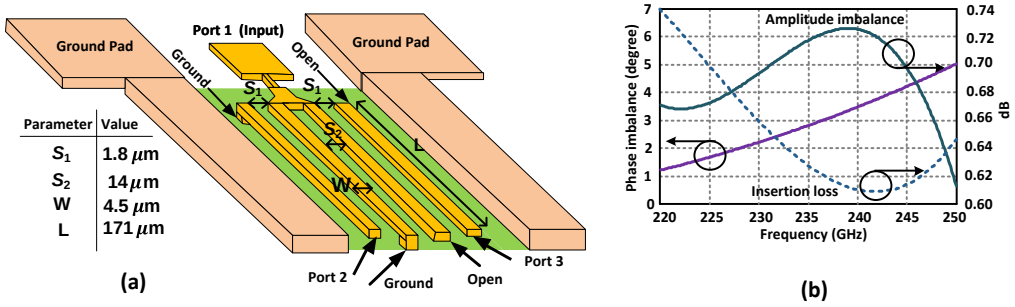
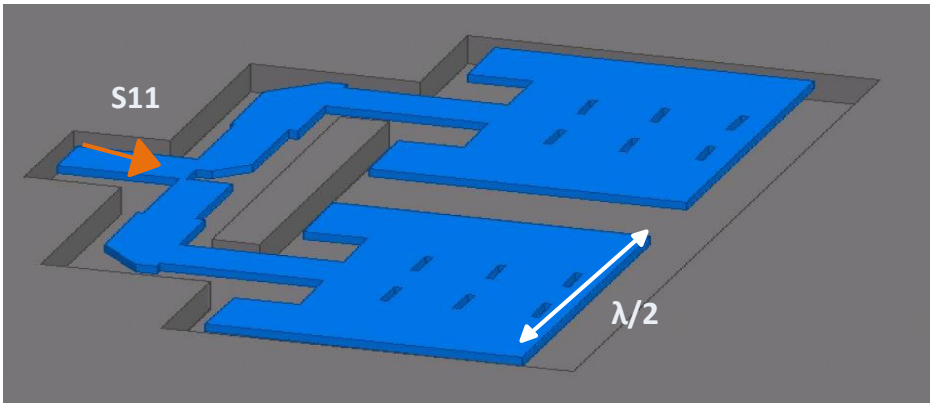


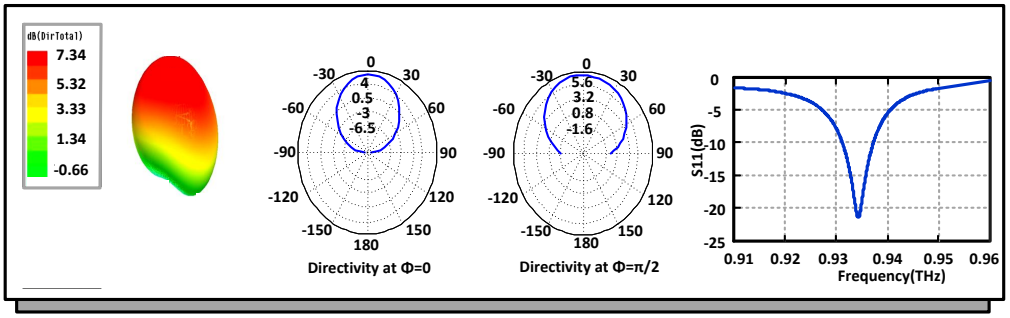
Figure 2.13: (a) the layout of the input balun and (b) the performance summary of the microwave short-open structure.

2.4.6 Output Power Extraction

The generated harmonic power of the frequency multiplier has to be extracted using an efficient scheme. In practice, there are two major techniques for THz wave measurement: 1) Design of low-capacitance pads and probing the output signal and, 2) radiation of the THz wave with an on-chip antenna. The probe solution faces challenges in terms of designing low-loss pads (due to the substrate capacitance) and the sensitive performance of the probe. However, by probing, a wideband measurement is feasible due to the broad transmission S_{21} profile of the THz probes. The alternative to the probing solution is the wave radiation. By approaching THz frequencies, the substrate thickness and wavelength



(a)



(b)

Figure 2.14: (a) the layout structure of the patch antenna array and (b) the simulated performance summary of the radiator.

become comparable and energy is lost in substrate modes. Extra wafer thinning and matched silicon lens are utilized to cancel the unexpected substrate loss [46],[58], [64]. However, in this design, to avoid this issue, a two-element patch antenna array with broad-side radiation from the top of the chip is utilized as shown in Fig. 2.14. Due to the limited distance between the top metal layer and ground shield layer (< 5μm), the antenna bandwidth is limited. The simulated performance of the antenna is shown in Fig. 2.14 and 72% radiation efficiency at 960 GHz and 7.3 dBi of directivity are achieved. Since the characteristic impedance of patch antenna is high (100~200 Ω), an array of two antennas

is designed for a better matching.

2.5 Measurement Results

The chip prototype is fabricated in 0.13 μm SiGe:C BiCMOS technology from STMicroelectronics. The circuit contains the microwave balun, the input matching network, the frequency quadrupler and the patch antenna array. The chip occupies a small area (0.37 mm^2) as shown in Fig. 2.15 and drwas 3 mA of current from a 1.9V supply. The measurement setup is shown in Fig. 2.16. A

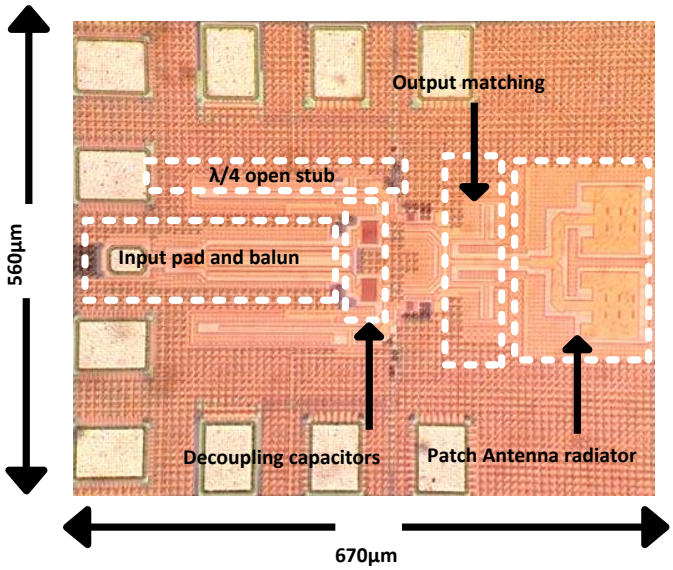


Figure 2.15: The die photograph

conventional measurement of THz radiators is by placing the receiver antenna at far field distance and approximate the transmitted power by using the Friis equation. In addition, the design of diagonal horn antennas is optimized for the coupling of plane waves [80]. However, the drawback of the far field measurement is the propagation loss which lowers the received power level significantly

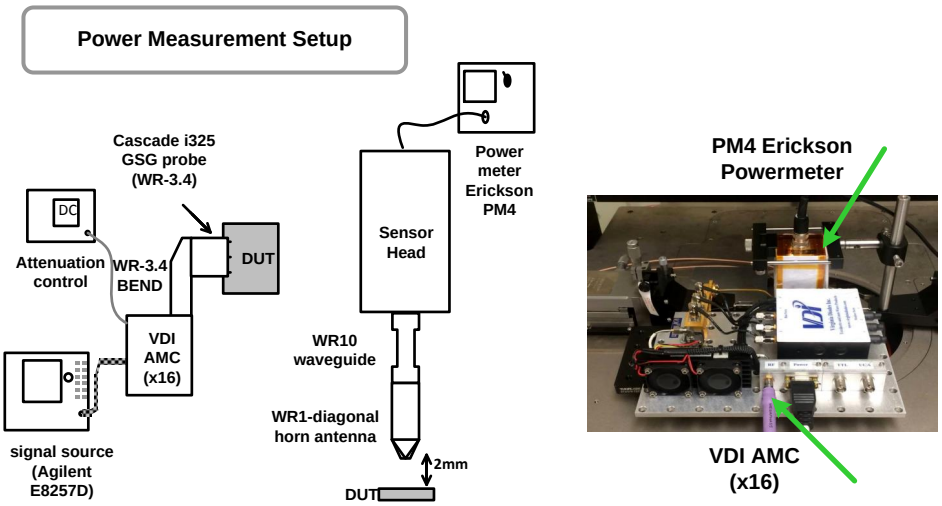


Figure 2.16: The implemented power measurement set up.

below the transmitted power ($\propto 1/d^2$).

For this chip, a near-field power measurement is performed due to the limited power and insufficient sensitivity of the power meter. As shown in Fig. 2.17(a), the WR-1 horn antenna at a spacing of 2mm on top of the radiator collects the radiation. Based on FDTD simulations with a precise EM solver, a power coupling efficiency of 9.8% is achieved (10 dB of power loss) for the 4th harmonic radiation from the chip to the input of the WR-10 waveguide in the near field measurement scheme. In addition, the WR-10 waveguide after the horn antenna adds a propagation loss of 1dB, measured using a VNA. Combined with the horn antenna coupling loss, a total power loss of 11 dB is considered. The rectangular waveguide of the horn antenna, enforces an exponential decay of lower harmonics radiation. On the other hand, the WR-10 waveguide passes the smaller wavelengths and in particular the THz wave. Moreover, as illustrated in Fig. 2.17(c), the simulated total radiated power of the 4^{th} harmonic is significantly higher than the other harmonics. This further guarantees that

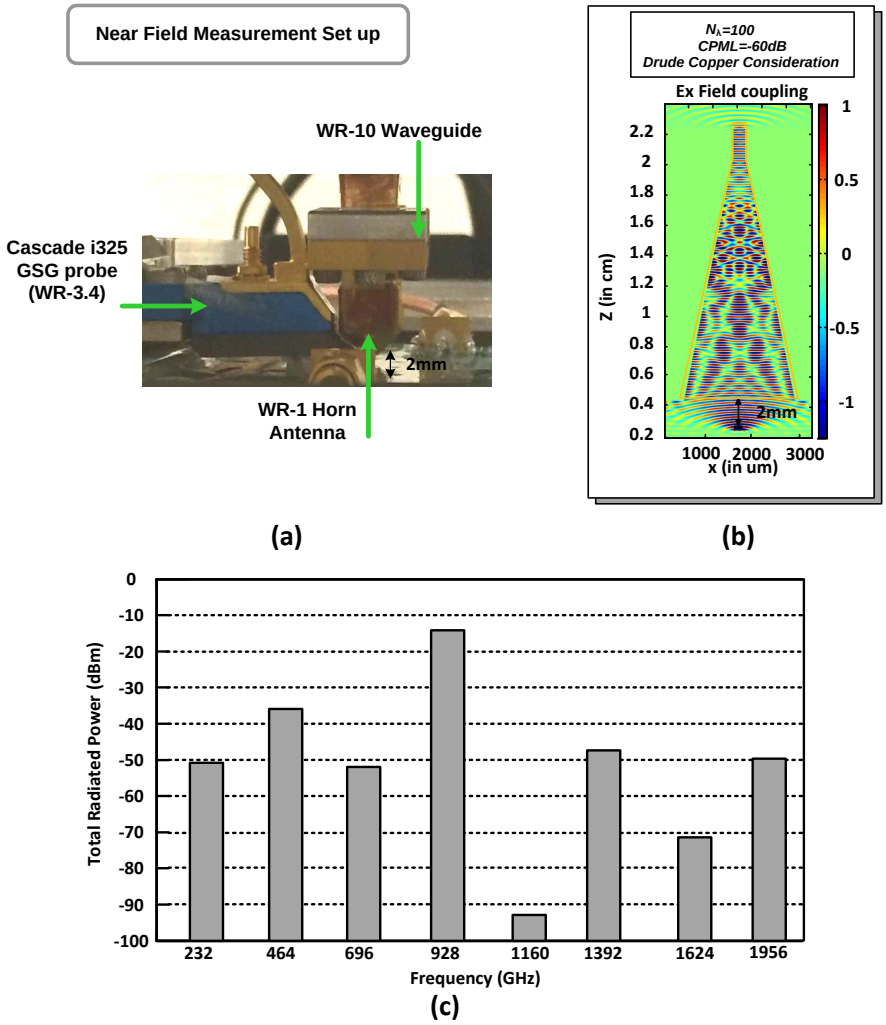


Figure 2.17: (a) the implemented near-field power measurement and (b) the diagonal horn antenna near field coupling (d=2mm), simulated by an accurate FDTD solver and (c) the simulated total radiated power at different harmonics for an input at 232 GHz.

the unwanted radiations are not coupled to the power meter.

One of the important considerations in measurement of THz waves is the characterization of the blackbody radiation. Therefore, to perform an accurate power measurement, the THz radiated power and the thermal emission should

be distinguished. The blackbody emission is in particular important when the silicon die is large and consumes a high DC power. In this measurement, we rely on an operational feature of the chip, which helps the calibration of the blackbody power. In principle, the quadrupler operation is divided into two different modes: "radiator on" and "radiator off" as shown in Fig. 2.18. Except the base voltage of Q_1 (VBase in Fig. 2.12), all the voltages are kept constant in the two cases. By changing the base voltage, the junction capacitors of Q_1 and the G and H coefficient are changed accordingly. However, due to the constant bias of the tail current source and the constant value of V_{dd}, the DC power consumption of the circuit does not change. On the other hand, the variation of the G and H coefficients changes the radiated power at the 4th harmonic by around 15 dB (Fig. 2.18(b)). Based on this phenomenon, by measuring the coupled power in the "radiator off" mode, the coupled power to the power meter is effectively the thermal radiation. In the "radiation on" mode, the coupled power to the power meter corresponds to the summation of the direct THz coupled power and the same blackbody emission. It is clear that the power difference of the two cases is not related to thermal variations as the power consumption is the same. As it is seen in the measurement results of Fig. 2.19, the coupled power exhibits a jump within the lower frequency band of measurement when the radiator is turned on and remains unchanged out of this band. This validates that the temperature variation is not the cause of these changes. Moreover, based on the bandwidth of the designed antenna, we expect to observe the THz power radiation in a limited bandwidth, which is also the case in our measurement. The simulated antenna with HFSS, has a slightly higher bandwidth which is due to the solution of the antenna based on the surface current components.

Taking into account the power coupling loss, the radiated power at differ-

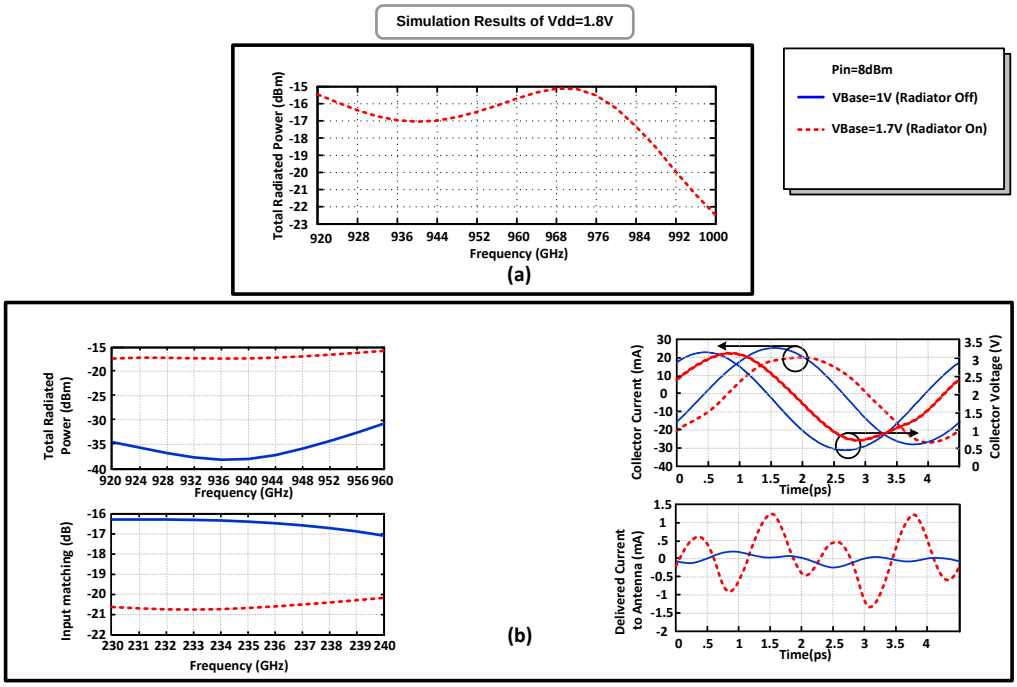


Figure 2.18: (a) Simulation results of the wideband power generation and (b) the circuit simulated operation in "radiator on" and "radiator off" modes.

ent frequencies is calculated. As shown in Fig. 2.19, the circuit radiates a peak power of -17.3 dBm at 0.928 THz and the antenna bandwidth will block the radiations above 0.944 THz. As we are exciting the input power from an external source by a probe waveguide and the power meter sensitivity is insufficient, the E/H plane radiation pattern measurement is not possible for this radiator. Therefore, based on the simulated antenna directivity (7.3 dBi), the circuit exhbits a peak equivalent isotropic radiated power of -10 dBm at 0.928 THz.

The output power radiation of this source is from 0.92-0.944 THz due to the limited bandwidth of the antenna. However, the quadrupler is in prinicple very wideband and exhibits only 8 dB of power variation within 80 GHz bandwidth (920 GHz to 1000 GHz) as the simulation results in Fig. 2.17 verify. According

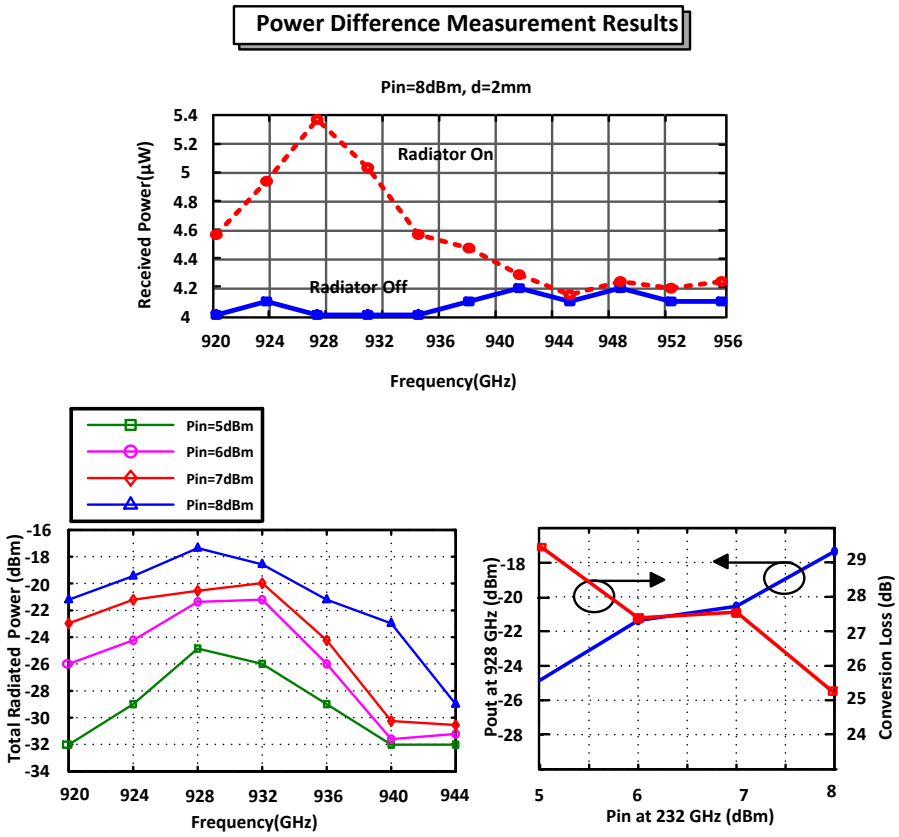


Figure 2.19: Measurement results. The power difference technique is utilized to measure all data points.

to Fig. 2.20, the design methodology introduced here, can boost the generated power and the operation frequency of electronic circuits. To the best of our knowledge, this circuit demonstrates the highest frequency radiator among all Si/SiGe sources. Table I, compares the performance of this THz power radiator with state-of-the-art Si/SiGe sources.

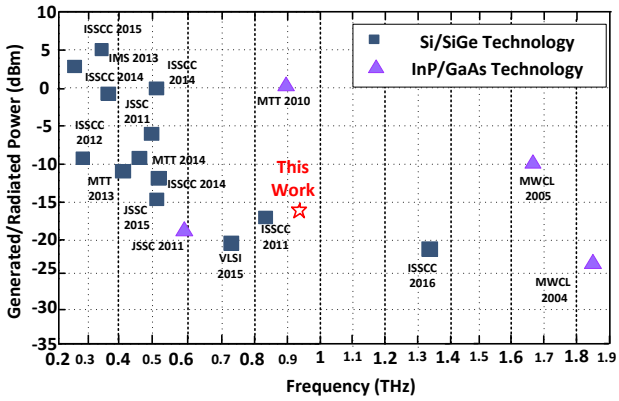


Figure 2.20: The performance summary of state-of-the-art THz sources.

2.6 Conclusion

In order to generate power at the higher end of THz frequency range, there are fundamental limits imposed by the existing technology. In order to extract the full potential of devices, an accurate model of power generation at the harmonics of the operation frequency ($f_0 < f_{max}$) is required. In this work, we propose a novel nonlinear model of harmonic power generation in electronic circuits which can be used in THz circuits. Based on the introduced model, a 0.92-0.944 THz frequency quadrupler is designed which demonstrates a radiated power level that is beyond the reach of conventional circuits. The proposed design methodology paves the path towards higher power generation as well as reaching higher operational frequencies.

Table 2.1: Comparison with state-of-the-art

Reference	Technology	Source type	Output Freq (GHz)	Generated Power (dBm)	Conversion Loss (dB)	Pdc (mW)	EIRP (dBm)	Remarks
This work	130 nm SiGe	Quadrupler	920-944/ 920-1000*	-17.3	25.3	5.7	-10 **	Radiator/ no lens
JSSC 2011 [11]	250 nm InP HBT	Oscillator	573	-19.2	15.35	115	NA	NA
MTT 2010 [12]	Planar GaAs Schottky diode	Multiplier	840-900	1.4	15.35	NA	NA	NA
ISSCC 2011 [38]	250 nm SiGe	Multiplier	820-845	-17	NA	3700	NA	Radiator/no lens
MTT 2013 [48]	45 nm CMOS	Quadrupler	390-440	-10	19.5	700	3	Radiator/ Quartz sub.
ISSCC 2015[55]	130 nm SiGe	Oscillator	320	5.18	NA	610	22.5	Radiator/ with lens
JSSC 2011[56]	90 nm BiCMOS	Oscillator	480-510	-16.6	NA	400	NA	Probed
JSSC 2011[57]	65 nm CMOS	Oscillator	482	-7.9	NA	61	NA	Probed
ISSCC 2012[58]	45 nm CMOS	Oscillator/ doubler	270-280	-7.2	NA	810	9.4	Radiator/ no lens
VLSI 2015[72]	65 nm CMOS	Quintupler	650-730	-21.3	33.8	0	-22	Radiator/ no lens
ISSCC 2016[73]	65 nm CMOS	Multiplier	1290-1440	-22.7	40	0	-13	Radiator/ no lens

* The first frequency range is from measurement which is limited by the input frequency range. The second frequency range is based on simulation.

** Based on simulated far-field antenna directivity

2.7 Analytical study of ratio functions

In this section, we show how the variations of device embedding in the simple circuit of Fig. 2.4(a) can impact the ratio functions. Based on the results of these analyses, the reader may conclude that the analytic derivation of ratio functions in some circuits might not be straightforward and simpler approaches similar to Section. II can be used. For simplicity, we consider the case of loss-less transmisssion lines since they can be designed to exhibit a high quality factor.

We assume an input power source with delivered power of P_0 and a corresponding voltage of V_S across a source impedance of Z_{0S}. There are two possi-

bilities for the base transmission line, TL_1.

2.7.1 No reflection from source

This case happens when the input line impedance is identical with the source internal impedance, i.e.,

$$Z_{0L_1} = Z_{0S}, \tag{2.22}$$

which leads to $\Gamma_s = 0$. The amplitude of fundamental voltage at the base of transistor (V_{in1}) is expressed in terms of load reflection coefficient, i.e.,

$$V_{in1} = V_{inL1} = V_0^+(1 + \Gamma_L), \tag{2.23}$$

where

$$\Gamma_L = \frac{Z_{inL1} - Z_{0L1}}{Z_{inL1} + Z_{0L1}}, \tag{2.24}$$

$$V_0^+ = V_S \frac{Z_{inS}}{Z_{inS} + Z_{0S}}. \tag{2.25}$$

This voltage will generate output fundamental voltages of V_{out1} and V_{out2} where,

$$V_{out,1} \simeq jZ_{0L_2} V_{in,1} G_{11} \tan(\beta_1 L_2), \tag{2.26}$$

$$V_{out2} \simeq jZ_{0L_2}(V_{in,1}^2 G_{12} + H_{12} V_{out,1}^2) \tan(\beta_2 L_2). \tag{2.27}$$

It is noteworthy that β_1 and β_2 are the propagation constants at the 1^{st} and 2^{nd} harmonic, respectively. The output harmonic voltage will generate an input current at $2f_0$ by the linear feedback admittance, i.e.,

$$V_{in2} = Z_{inL1@2f_0} Y_{12@2f_0} V_{out,2}. \tag{2.28}$$

According to (28)-(32), the ratio functions can be found in terms of the device properties and the embedding network parameters. By changing the length of

TL_1, the phase of $V_{in,1}$ changes according to (30). This phase variation is linear up to the first order and is equal to $\beta_1 \Delta L_1$ which results in the same phase variation at $V_{out,1}$. However, the second harmonic voltages are determined by second power of V_{in1} and V_{out1}; hence, their phases change by $2\beta_1 \Delta L_1$. Similarly for any higher harmonic n, the phase of harmonic voltages change by $n\beta_1 \Delta L_1$. In addition, for a limited range of variations on the length of transmission lines, the amplitude of (30) does not change significantly and the amplitude of voltages can be approximated as constants. Therefore, by changing the length of TL_1, the amplitude of second harmonic ratio functions R_2 and S_2 are almost preserved; however, their phases change by $\beta_1 \Delta L_1$. Fig. 2.21 (b) illustrates the simulated amplitude and phase of input and output voltages which match with the theory.

On the output side, by changing the length or Z_0 of TL_2, the output voltages V_{out1} and V_{out2} change according to (31) and (32). In addition, the second harmonic voltage at the input V_{in2} changes according to (33). Finally, the fundamental voltage at the input V_{in1} changes according to (29) where the input impedance is impacted by the variations of the load impedance, i.e.,

$$Z_{inL1} \simeq \frac{1}{Y_{11}} \| \{ \frac{-G_{11}}{Y_{11}H_{11} - Y_{12}G_{11}} + Z_L \| \frac{1}{H_{11}} \}, \tag{2.29}$$

where the Y parameters of the transistor and the load impedance of $Z_L = jZ_{0L2} \tan(\beta_1 L_2)$ appear. Since the trigonometric functions operate differently at f_0 and $2f_0$ in (31) and (32), the amplitude and phase of output ratio functions change this time. Similarly, according to (31) and (32), the amplitude and phase of ratio functions at the input port also change. Fig. 2.22 illustrates the amplitude and phase variations of fundamental and harmonic voltages as well as the ratio functions.

2.7.2 Reflection from the source

This condition happens when the the internal impedance of the source Z_{0s} and the characterisitc impedance of the base transmission line TL_1 are different. This condition is undesired if the source reflection leads to a poor power delivery at the fundamental frequency. However, we would analytically consider the slight variations from the identical Z_0S. More importantly, the relative phase and amplitude of fundamental and harmonic voltages can change differently in this case which could lead to a higher harmonic power.

As it is shown in [78], for this case V_0^+ is impacted by $\Gamma_S = \frac{Z_{0s}-Z_{0L1}}{Z_{0s}+Z_{0L1}}$, i.e.,

$$V_0^+ = V_S \frac{Z_{0L1}}{Z_{0S} + Z_{0L1}} \frac{e^{-j\beta_1 l}}{1 - \Gamma_L \Gamma_S e^{-2j\beta_1 l}} \tag{2.30}$$

By combination of (28) and (35), the fundamental input voltage is determined. In this case, the length variation of TL_1 impacts the amplitude and phase of the fundamental voltage V_{in1} significantly. By applying (31)-(33), the amplitude and phase variation of other voltage components are also determined. The results in Fig. 2.23 illustrate the simulated ratio functions for this case.

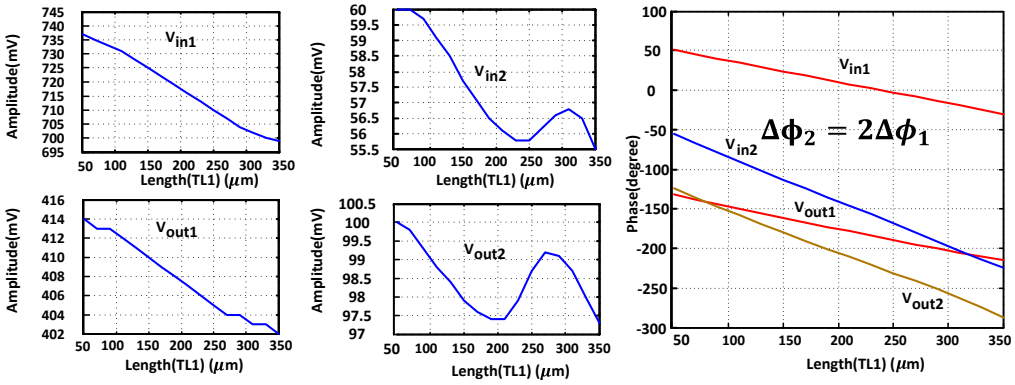


Figure 2.21: The simulated variation of amplitude and phase of input and output voltage components by variations of length of TL_1.

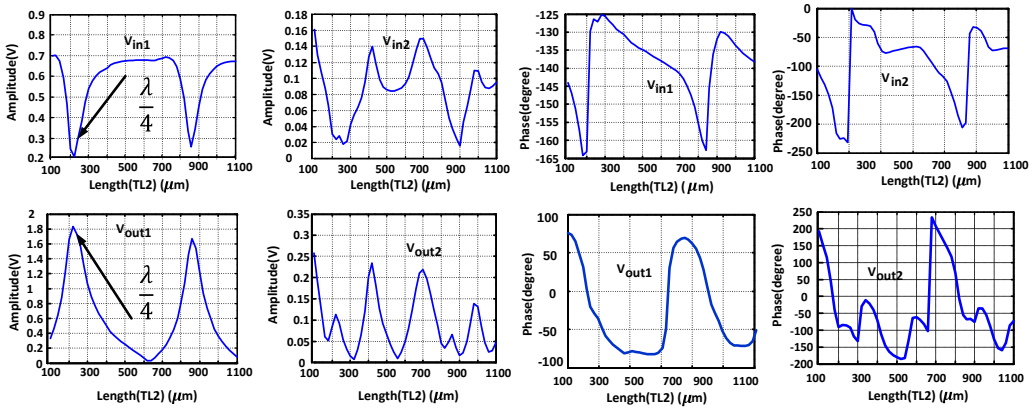


Figure 2.22: The simulated variation of amplitude and phase of input and output voltage components by variations of length of TL_2.

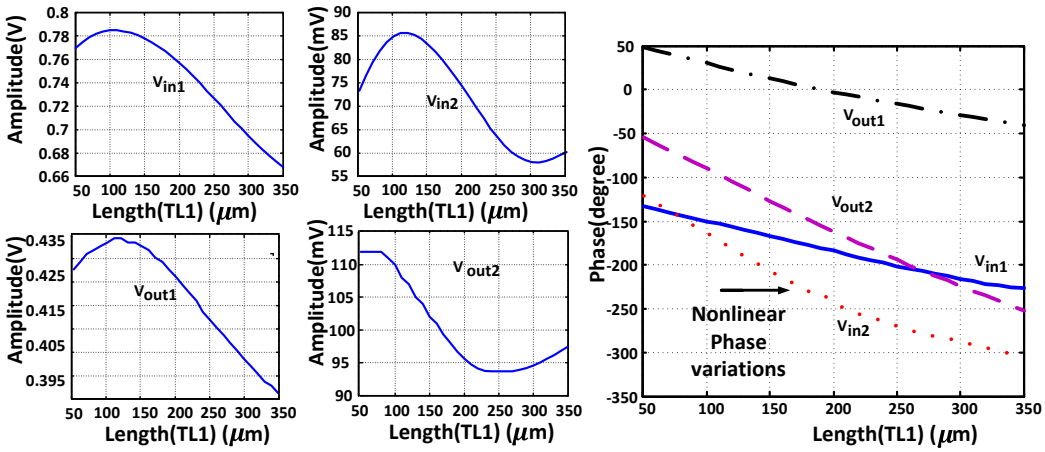


Figure 2.23: The simulated variation of amplitude and phase of input and output voltage components by variations of length of TL_1 when there is source reflection.

CHAPTER 3

A 0.43-0.51 THZ SIGE FREQUENCY DOUBLER BASED ON THE NONLINEAR HARMONIC GENERATION THEORY

3.1 Introduction

Emerging applications of the THz range (0.3-3 THz) include different areas of interest, e.g., molecular spectroscopy, high resolution imaging and ultra-fast communication. To demonstrate THz transmitters, mW order of power should be generated in order to battle the high propagation loss in this frequency range. However, there are different challenges to reach the required power, e.g., the lower power gain of the active devices and the lower quality factor of passive components.

The two conventional schemes of power generation at the THz range are: 1) extraction of power from a harmonic VCO [62] and 2) conversion of high power fundamental signals to the desired harmonic through a chain of frequency multipliers. Although the former technique exhibits a simpler design, the limited tuning of oscillators makes the second scheme more favorable.

Previously, frequency multipliers have been demonstrated at the THz range. However, the bandwidth of operation and saturated output power in most cases are not sufficient. In this work, a nonlinear model to characterize the active device and maximize the output harmonic power is introduced. Using a 130 nm SiGe technology, this work demonstrates the highest frequency among active multipliers and the highest bandwidth among all sources above 300 GHz.

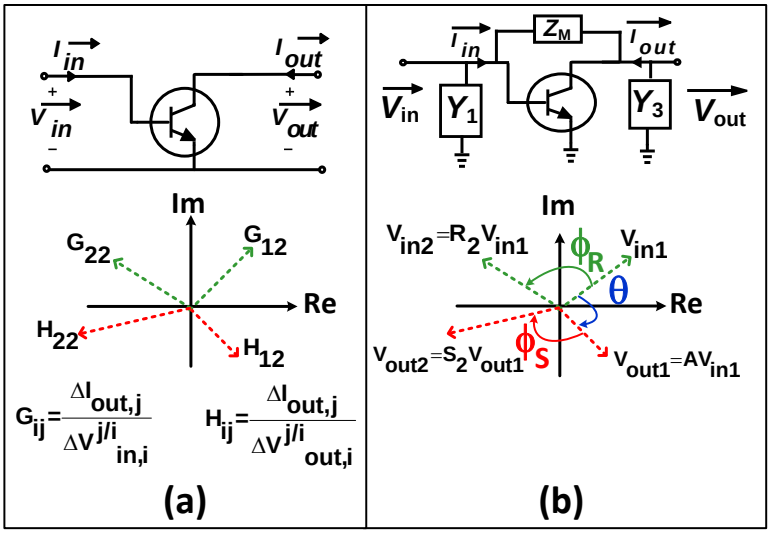


Figure 3.1: (a) The transistor operators of harmonic generation and (b) the impact of passive network.

3.2 Nonlinear Model of Harmonic Generation

In order to maximize the harmonic power, all the mechanisms that generate the power at the harmonic of interest should be considered. Based on the Volterra-Weiner theory of nonlinear devices [72], the active device is characterized by nonlinear and linear operators, as depicted in Fig.3.1. The G_{ij} and H_{ij} operators represent the gain from the i^{th} harmonic of the voltage at the input and output ports to the j^{th} harmonic of the output current, respectively. For identical i and j the operators are linear, otherwise they are nonlinear. By neglecting the small intermodulation operators at the operation frequency, the 2^{nd} harmonic current can be written as,

$$I_{out,2} = G_{1,2}V_{in,1}^2 + H_{12}V_{out,1}^2 + G_{22}V_{in,2} + H_{22}V_{out,2}. \tag{3.1}$$

Moreover, the real power generated at the 2^{nd} harmonic can be written as,

$$P_{out,2} = Re\{I_{out,2}V^*_{out,2}\}. \tag{3.2}$$

As illustrated in Fig. 3.1(b), by placing the transistor in a linear embedding network, the linear operators change accordingly and the nonlinear operators remain unchanged [72]. For any selected circuit topology, the amplitude (A) and phase (θ) of fundamental voltage gain, as well as the ratio of the second harmonic to fundamental voltage components ($R_2e^{j\Phi_R}$ and $S_2e^{j\Phi_S}$) are determined. For an invariant circuit topology (invariant passive network with variable values, constant bias conditions and invariant transistor), by changing the values of the passive components, A and θ change easily. However, the harmonic ratio values exhibit very small variations and are considered as constants. Therefore, for a particular circuit topology, the current expression in (1) can be approximated as,

$$I_{out,2} \simeq G_{1,2}V^2_{in,1} + H_{12}V^2_{out,1} + G_{22}\vec{R_2}V_{in,1} + H_{22}\vec{S_2}V_{out,1}, \tag{3.3}$$

where $\vec{R_2} = R_2e^{j\Phi_R}$ and $\vec{S_2} = S_2e^{j\Phi_S}$.

By substitution of $V_{out2} = S_2V_{out1}$, the 2^{nd} harmonic power expression in (2) is represented as a nonlinear function of the fundamental voltage components. Therefore, by changing the values of the passive components, the optimum conditions of the harmonic power generation are determined in terms of A and θ. It is noteworthy that this nonlinear power expression, is different from the linear power optimization in [62].

3.3 Circuit Design and Optimization

The schematic of the multiplier circuit is shown in Figure .3.2. To take the maximum benefit from the nonlinear profile, a differential common-emitter circuit is used in this design. For a stable operation, MOS tail current sources are used. However, the impact of degeneration on the nonlinear profile should be minimized. Therefore, tail current source impedance is bypassed with custom finger capacitors $C_1 \simeq 40fF$. Furthermore, TL_3 with $Z_0 = 40\Omega$ shrinks the capacitive impedance looking from the base and effectively a small real impedance is seen at the emitter node.

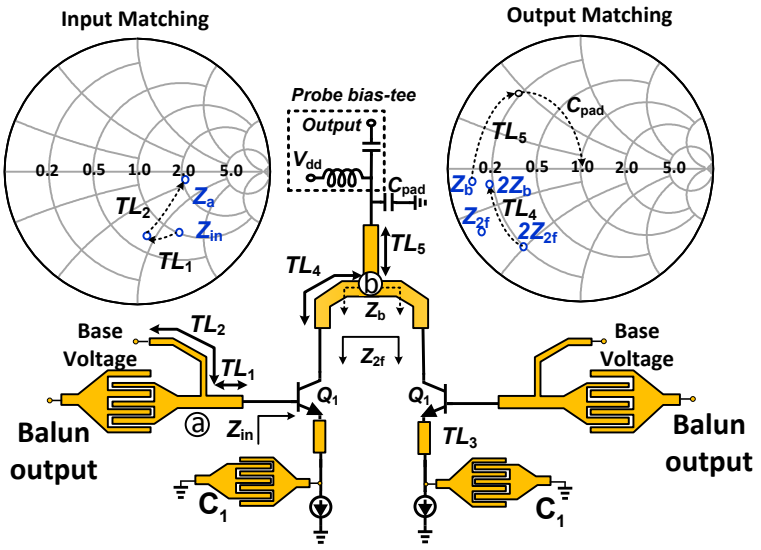


Figure 3.2: Schematic of the active doubler and the input/output matching scenarios on smith chart

The transmission lines TL_1, TL_2, TL_4 and TL_5 should satisfy the optimum power matching conditions. As shown in Figure 3.2, the combination of TL_1 and TL_2 transforms the impedance seen at node "a" to real part of 100Ω. The low-loss (S_{21}=-0.6dB) finger capacitors are designed to reach zero imaginary

around the input operation frequency. Therefore, they act as almost ideal decoupling capacitors within a sufficiently large bandwidth. Since the two balun output nodes are matched to the 50Ω input impedance, a wideband fundamental matching at the input is performed, as shown in Figure 3.3(a). In addition, inductor of TL_1 and C_π of Q_1 form a local resonator which increases amplitude of $V_{in,1}$.

3.3.1 Wideband Operation

Due to the differential operation of the circuit, the fundamental components reaching node "b" are out of phase and form a virtual ground which reflects them back to the transistors. However the in-phase 2^{nd} harmonic components have to be matched to the output port. As shown in Figure 3.2, TL_4 and TL_5 translate the impedance Z_{2f} to an impedance with real part of 50Ω and an inductive imaginary part. Using the output pad capacitance (C_{pad}), the output is matched to 50Ω within a wide range, as shown in Figure 3.3(b). Between, the different combinations of TL_4 and TL_5 the one that reaches the maximum fundamental swing and provides the fundamental optimum Φ are selected, i.e., TL_4 = 60μm and TL_5 = 90μm.

One of the major features of this active circuit is the bias manipulation to increase the power and bandwidth. In particular, by changing the base voltage of Q_1, the junction capacitors and subsequently the G operators change. As illustrated in Figure 3.4(a), the bias manipulation provides a high 3-dB bandwidth of 80 GHz. Moreover, for a fixed frequency, by varying the power level, the maximum power generation is achieved by the base bias manipulation, as shown in

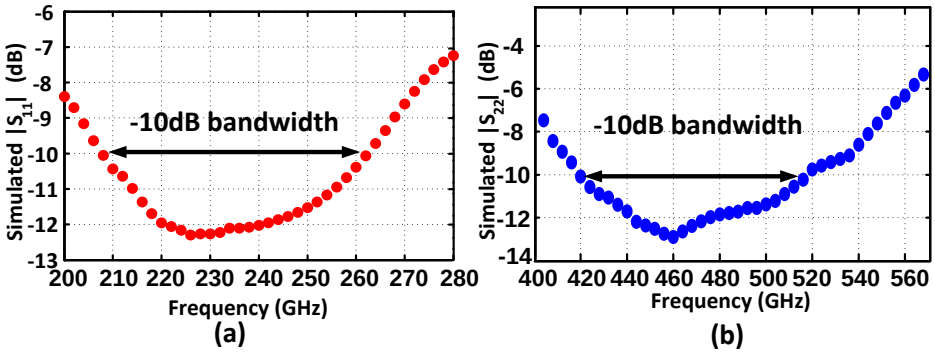


Figure 3.3: Wideband matching at (a) input and (b) output

Figure3.4(b).

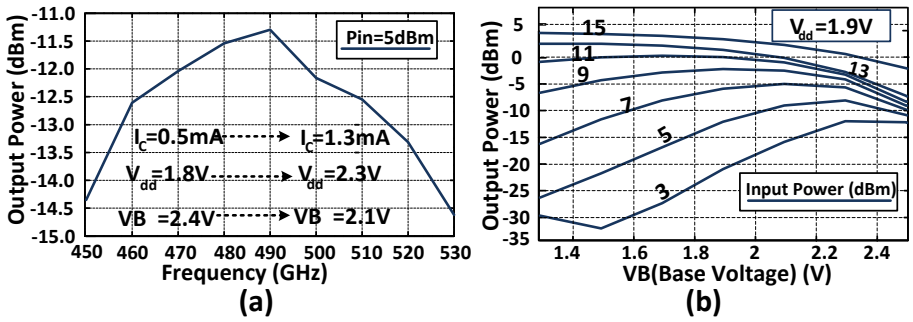


Figure 3.4: Using bias manipulation technique for (a) wideband power generation and (b) maximum power generation at a fixed frequency.

3.3.2 Differential Signal Generation

To generate a differential power from the single-ended external source, a microwave balun is required. The selected balun should exhibit a wideband operation. Moreover, the conversion loss should be minimized to deliver the maximum power to the doubler. Finally, the selected balun should match with the

layout pattern imposed by the rest of the circuit. Therefore, a microwave passive short-open balun is designed as shown in Figure 3.5. The capacitive coupling of the adjacent transmission lines with proper terminations, leads to out of phase signal coupling at ports 2 and 3. As depicted in Figure 3.5(b), this balun preserves the phase/amplitude balance as well as a low conversion loss (< 0.8dB) within a large bandwidth.

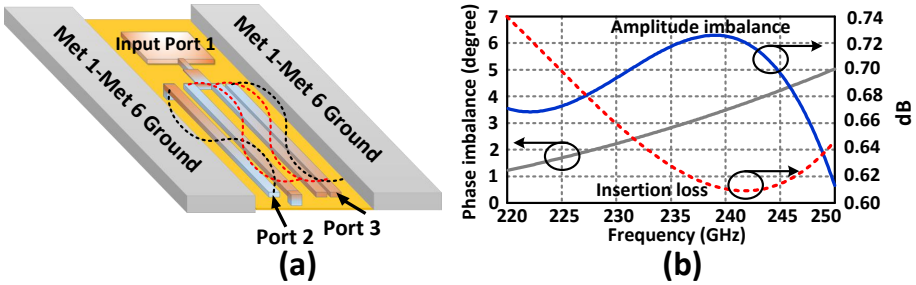


Figure 3.5: (a) 3D illustration of the input pad and balun and (b) the insertion loss and phase/amplitude imbalance simulated by HFSS

3.4 Experimental Results

The doubler is fabricated in 130 nm SiGe BiCMOS technology from STMicroelectronics. The chip photograph is shown in Figure3.6(a). The circuit occupies a small area of 0.36 mm^2 and consumes a maximum DC power of 5.7 mW. The measurement setup is shown in Figure3.6(b,c). The VDI AMC (X16) amplifier/multiplier chain generates the input power within the limited bandwidth of 230-240 GHz. The additional measured loss of WR-3.4 bend waveguide and the WR-3.4 probe adds attenuation to this value; hence a maximum power of 8dBm is delivered to the circuit. On the output side, the WR-2.2 probe is used for both power extraction and biasing the chip with the internal bias-tee.

The waveguide in this probe fully rejects the components below the cut-off frequency, including the fundamental signal. Moreover, the simulated power of the 3^{rd} harmonic is 25 dB lower than the second harmonic. Therefore, the output power in this measurement is ensured to be related to the second harmonic component.

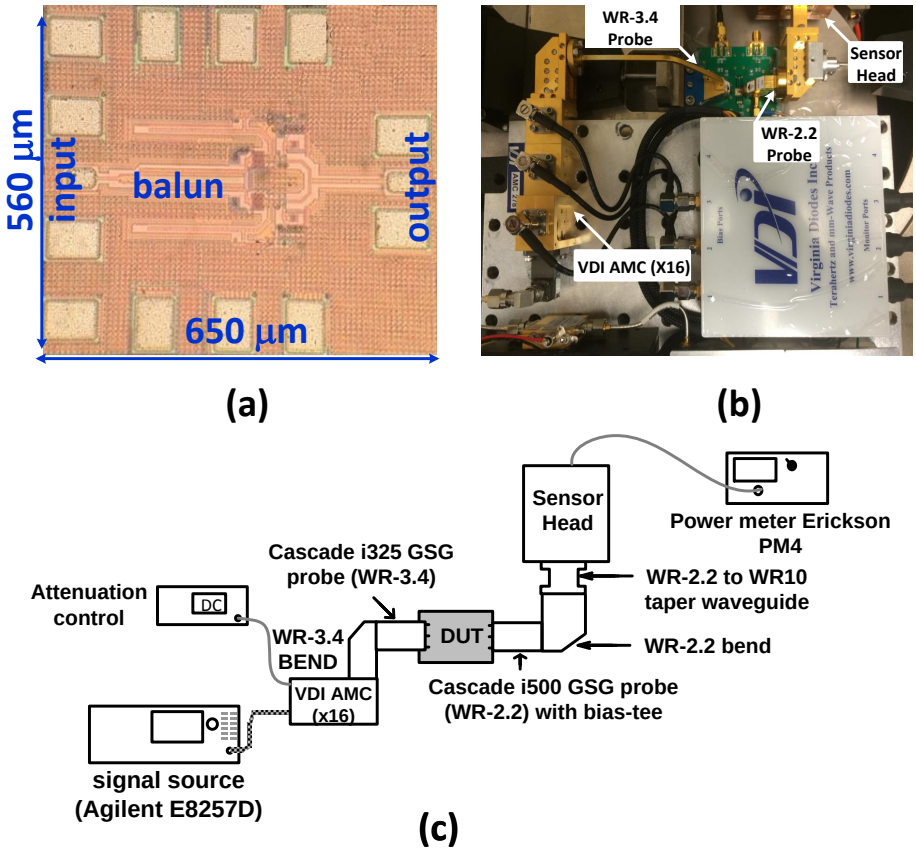


Figure 3.6: (a) the die photograph, (b) and (c) the measurement set up.

In Figure 3.7, the measurement and simulation results for an input power level of 5dBm are compared. The input power level is controlled by the attenuation control of the VDI source. Using the bias manipulation technique,

Table 3.1: Performance Comparison of Solid State Sources

Reference	[62]	[55]	[?]	[?]	[8]	[?]	**This Work**
f_{out} (GHz)	482	325	480	180	317	390	480
Type	oscillator	active x2	passive x2	active x2	oscillator	oscillator	active x2
P_{out} (dBm)	-7.9	-3	-6.3	0	5.2	-26.6	-8.2
CL(dB)	N/A	6(gain)	14.3	6.4	N/A	N/A	16.2
3-dB BW	0	6.3%	14.6%	11.1%	N/A	2.2%	† 16.6%(sim)
P_{dc}(mW)	61	24	0	39	610	21	5.7
Technology	65 nm CMOS	130-nm SiGe	65 nm CMOS	45 nm CMOS	130 nm SiGe	40 nm CMOS	130 nm SiGe

† Due to the limited bandwidth of the input source, the full 3-dB bandwidth could not be measured.

the output power changes by only 0.8dB, within the 20 GHz measured output bandwidth, which declares the wideband characteristic of the circuit.

In Figure 3.8, the simulation and measurement results of the doubler response to power sweep at 240 GHz are illustrated. Based on the simulation results, this active circuit, exhibits a high saturated power level of 4 dBm and conversion loss variation of 5.5 dB within 25 dB variation of input power. In measurements, due to the limited power of the input source, the maximum output power of -8.2 dBm is achieved for an input power of 8dBm.

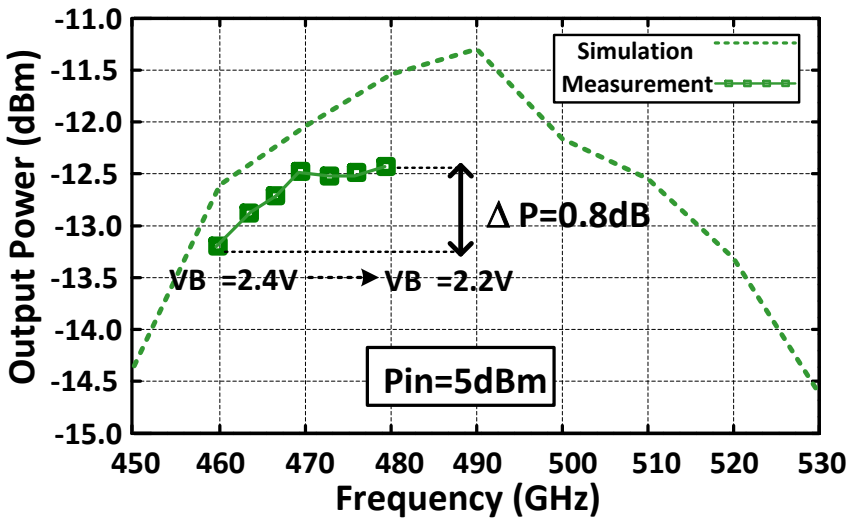


Figure 3.7: Simulation and measurement results for an input power of 5dBm.

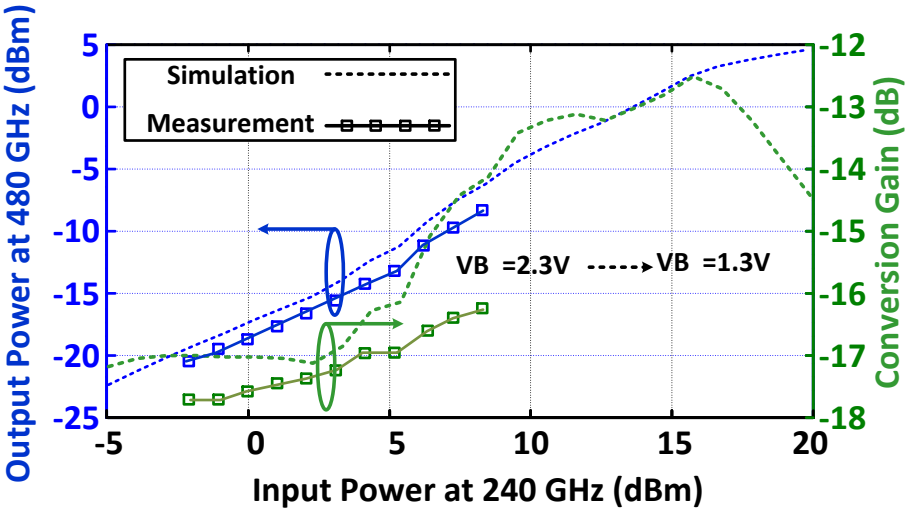


Figure 3.8: Simulation and measurement results of operation at 240 GHz for different power levels.

CHAPTER 4

SMART DETECTOR CELL: A SCALABLE ALL-SPIN CIRCUIT FOR LOW-POWER NON-BOOLEAN PATTERN RECOGNITION

HOLLISTIC APPROACHES TO DESIGN HIGH SPEED ELECTRONIC CIRCUITS

Hamidreza Aghasi, Ph.D.

Cornell University 2017

Abstract—We present a new circuit for non-Boolean recognition of binary images. Employing all-spin logic (ASL) devices, logic comparators and non-Boolean decision blocks for compact and efficient computation are designed. By manipulation of fan-in number in different stages of the circuit, the structure can be extended for larger training sets or larger images. Operating based on the mainly similarity idea, the system is capable of constructing a mean image and compare it with a separate input image within a short decision time. Taking advantage of the non-volatility of ASL devices, the proposed circuit is capable of hybrid memory/logic operation. Compared with existing CMOS pattern recognition circuits, this work achieves a smaller footprint, lower power consumption, faster decision time and a lower operational voltage.

4.1 Introduction

Pattern recognition and in particular, image recognition techniques have been widely studied in machine learning and image processing [84, 85, 86]. Hardware demonstration of computation units for pattern recognition; however, has consistently been a challenging problem in terms of chip size, power consumption, computation complexity and decision speed.

Among different solid state technologies, CMOS provides the chance of low cost, highly-integrated low power implementation for pattern recognition [88, 89, 87, 90] and processing [91, 92] systems. For boolean logic systems, CMOS gates exhibit processing speeds up to a few GHz and can be designed to have a low static power. However, the dynamic power consumption of a large system with a GHz clock frequency can still limit the scalability. Fan-in and fan-out considerations for CMOS devices also impact the speed, power consumption and the size of devices. Besides boolean systems, some novel non-Boolean techniques have been developed to overcome these issues. In non-Boolean systems, logic gates will no longer be the key block and analog/mixed signal circuits are used. In [89], the authors propose a technique for non-Boolean training and detection of image pixels using a network of coupled oscillators. This structure has the capability to detect any scaled or rotated version of a desired image. On the other hand, this method suffers from high computational complexity, large area and high power consumption which limit the application for large image arrays. To this, we should also add the long convergence time. Other proposed CMOS systems have demonstrated artificial neural networks (ANN) by designing circuits emulating neurons and synapses [88, 87]. In these systems, the larger computation burden, leaves the search open for new solutions.

To overcome the limitations of CMOS devices, other technologies are being investigated for pattern recognition applications. Spintronic devices, in particular, have received a lot of attention recently because of some unique properties, e.g., low voltage operation and non-volatility. In [93], a non-volatile logic-in-memory full adder is fabricated using the magnetic tunnel junctions (MTJ). The proposed architecture is compared with an 0.18μm CMOS process counterpart and exhibits major advantages. The dynamic power consumption compared to a conventional CMOS circuit is reduced by 23% due to reduction in the number of paths from V_{DD} to GND. On the other hand the static power consumption is eliminated due to the non-volatility and the chip area is smaller.

As shown in [94], the ASL devices are also non-volatile and the conputational state is preserved when the power to the circuit is turned off. In [95], a spin-based artificial neural network (ANN) is proposed using lateral spin valves to achieve a low power consumption and a low operatoinal voltage. In [96], spin swithces to develop compact neurons and synapses are proposed. In [97], all-spin logic (ASL) and charge-spin logic (CSL) devices are shown to be capable of Boolean and non-Boolean operations which make them an attractive choice to build some fundamental blocks such as ring oscillators. In addition, the design of ASL gates with graphene channels have been proposed recently [**?**]. Due to the unique features of graphene in terms of the spin transport, the design of Boolean and non-Boolean computation units with these new devices can be investigated as a future direction.

The majority gate operation of ASL devices has been previously introduced in some Boolean logic systems [100, 102]. This unique feature of these devices can overcome fan-in and fan-out limitations of large integrated systems. Be-

sides, the inverting and non-inverting operation modes of ASL devices can be the key to design many logic circuits e.g., full adder circuits and multipliers [104]. The time domain transient behavior of magnetization in these devices also provides another degree of freedom to demonstrate non-Boolean operations. These features combined, enable us to design an all-spin logic non-Boolean compact structure with low power consumption and low computational complexity.

In this paper we propose a novel pattern recognition circuit that takes advantage of novel features of spintronic devices such as non-volatility, efficient implementation of majority gates and XOR functions and the ability to distinguish strong and weak majorities. Non-volatility of the devices enables storing large sets of training images within the logic with no standby power dissipation. This feature also enables instant-on operation and saves on energy and delay penalties imposed by loading training images from a main memory.

The rest of this paper is organized as follows. Section II describes the operation of ASL devices. The proposed approach and the basic of computation are given in Section III. In Section IV, the proposed architecture and a comprehensive discussion on design considerations are presented. Simulation results and summary are shown in Sections V and VI, respectively.

4.2 All-Spin Logic Devices

Spin of electron is introduced as a new state variable in spintronic devices to process and store information. This new alternative to charge-based systems, provides the possibility of achieving an ultra-low voltage operation and easier

demonstration of digital systems coming from the bistable nature of spin [98].

In all-spin logic devices, input and output data are represented by the magnetization of two ferromagnets [101] which are communicating through a spin-coherent metallic channel. The physical view of these devices is shown in Figure 4.2(a). As shown in the Figure 4.2 and discussed in [99], the applied voltage on the input ferromagnet, creates a flow of electrons which moves them from the supply voltage to the ground. This flow of electrons, becomes spin-polarized when passing through the input ferromagnet. Since the concentration of the spin-polarized electrons are different at the input side and the output side of the channel, the electrons diffuse to the output side. The accumulated spin-polarized electrons under the output ferromagnet, can switch the magnetization orientation of the magnet by applying a torque based on spin-transfer torque effect.

As shown in [100], these devices can be concatenable, exhibit nonlinear characteristics and support all Boolean operations. In all-spin logic operation, by using the direct spin signal, the nanomagnet can be switched and this signal can be transferred to the next stage. By storing the information in the spin magnetization of magnets, the input and output magnets can effectively be considered as digital capacitors linked by a spin-coherent channel. The sign and magnitude of control voltages applied on the magnets, determine the polarity of majority spin electrons and the device speed, respectively. Any change of magnetization in the bistable input magnet can exert a spin current through the channel and this current can determine the spin magnetization of the output magnet [101]. The channel between the two magnets can be either a metal or a semiconductor [106, 107, 108]. In our modeling and simulations we assume a copper intercon-

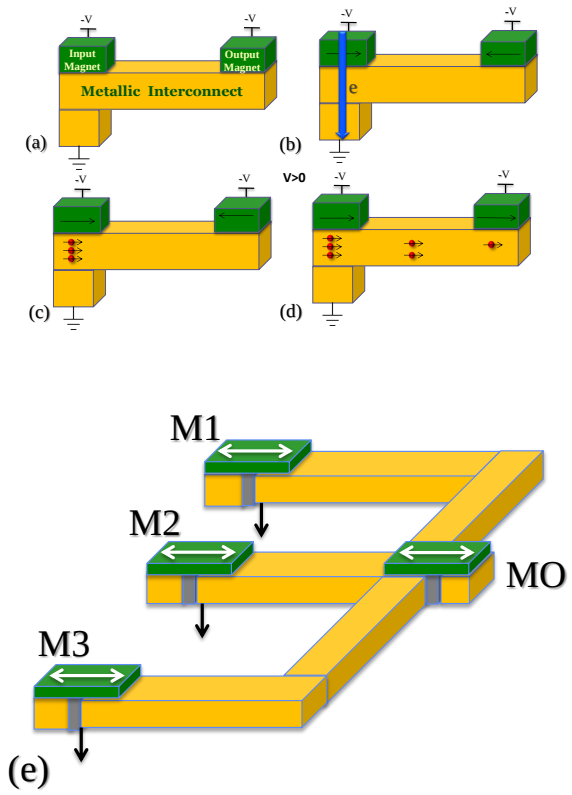


Figure 4.1: (a) Configuration of single ASL device (b) Applied voltage on the magnet, creates an electric field and enforces electron movements. (c) Spin-polarized electrons at the input side exhibit a higher density compared to the output side. (d) The diffusion of spin-polarized electrons towards the output magnet, changes the output magnetization direction. (e) An ASL Majority Gate with 3 inputs [101]. The 3 input magnets, M1, M2 and M3 are connected to the output magnet MO using 3 metallic interconnects.

nect.

The models utilized in this work are based on [101] where the different physical effects are captured. The accurate parameters of channel, magnet and interface that determine different performance characteristics, e.g., the spin injection,

detection and transport efficiency are taken into account. The most important size effect parameters for the purpose of this work are the side wall specularity, the grain boundary reflectivity and the average grain size [99]. The average grain size is assumed to be equal to the width of thickness of the metals [99]. The complete list of parameters is in Appendix B.

4.2.1 Majority Gate Operation

As mentioned earlier, the ASL device supports a majority operation as shown in Figure 4.1(e). This feature is achieved because the net spin current to the output magnet can be determined by the sum of all input spin currents from all the input devices. In principle, this system can be designed for large number of inputs. As a trade off, by increasing the number of input devices in a majority gate, the uncorrelated thermal noise of these devices add up and impact the transient magnetization of output magnet, thus we need to make sure that in this design we have the proper fan-in. As it will be discussed later, if we only want to monitor the final steady value of the output magnetization, we can keep increasing the number of input devices as far as the output magnetization is predictable. Based on the device properties, this phenomenon sets a practical limit on the number of input devices to a majority gate. On the other hand, if we care about the transient behavior of the output magnetization, fewer inputs should be connected to the output magnet to avoid the noise accumulation of input devices. In our simulations, for 3 and 5 input cases, the transient output magnetization is less impacted by the thermal noise, compared to higher fan-in numbers. We have to clarify that the steady state value of the majority gate depends on the sign of applied voltage on the magnets. In case of having

a negative voltage applied on the magnets, the magnetization orientation value will finally be the exact majority of the input magnetizations. However, if the applied voltage is positive, the steady state value of the output magnet will be the complementary majority of the input magnetizations.

The interesting phenomenon in ASL majority gates rises from the dependency of the transient behavior of the output magnetization on the number of similar input magnetizations. This effect can be validated by the fact that the transferred spin torque increases when there are more magnets with magnetization in the same direction. Figure 4.2, shows the different scenarios of transient output magnetization in majority gates with 3 and 5 inputs. As shown in Figure 4.2(a), in a majority gate, with 5 inputs, the switching of output magnetization becomes faster when there are more inputs with similar magnetization directions. As the number of magnets with similar magnetization decreases, the switching happens slower and the effect of thermal noise is sensed more. In Figure 4.2(b), the switching transition for two majority gates with 3 inputs and 5 inputs are compared. By considering the fact that the thermal noise accumulation in the gate with 3 inputs is less compared to the gate with 5 inputs, in the case of having equal net spin currents to both gates, the gate with 3 inputs, exhibits more deterministic transition.

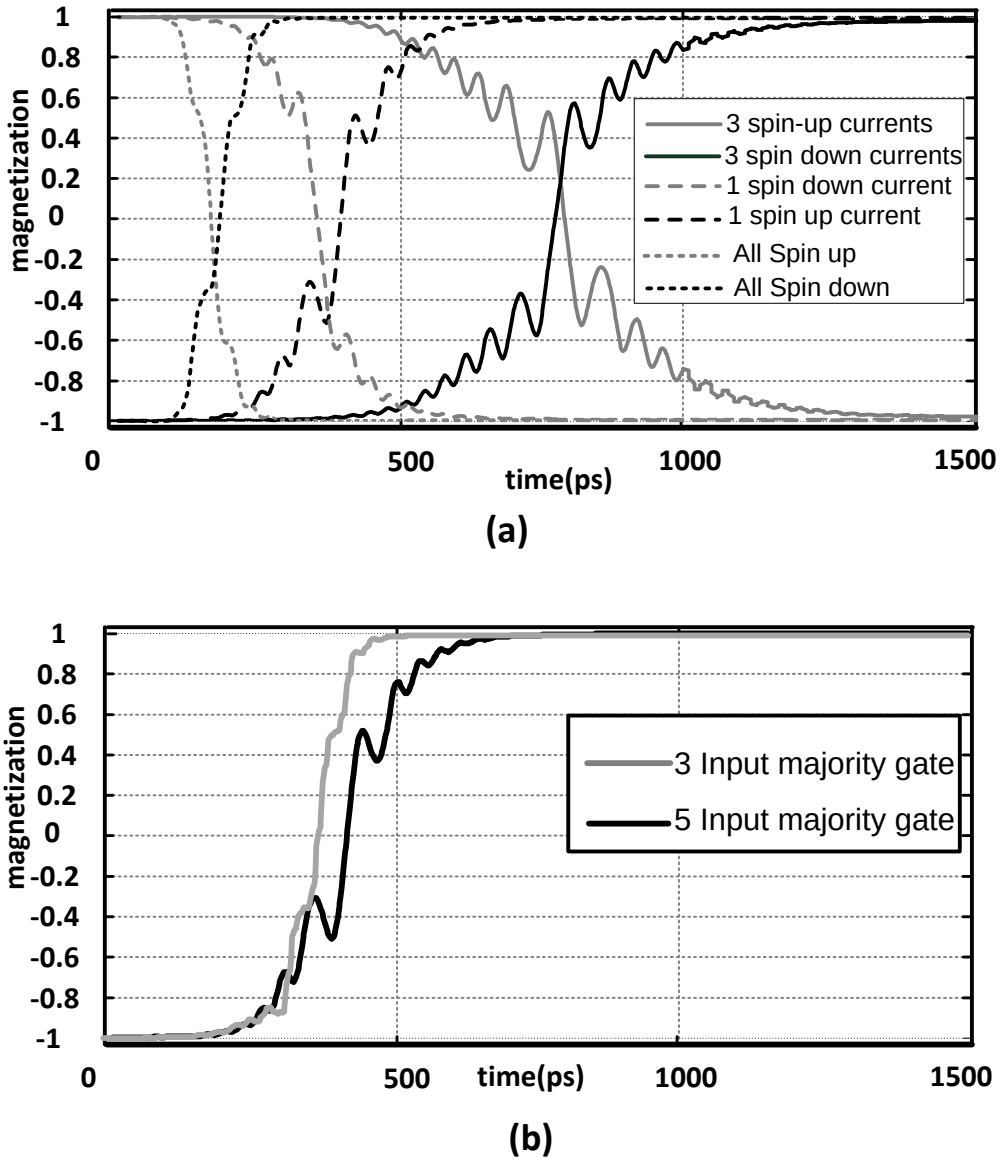


Figure 4.2: (a) Switching transient response for different scenarios of input magnetization in a majority gate with 5 inputs. (b) Switching transition comparison of majority gates with 3 and 5 inputs. In this comparison, the input magnetization of magnets to the 3 input gate are all similar. For the gate with 5 inputs, 4 inputs have similar magnetization and the net spin current is equal to the other gate. The applied voltage on the magntes in these simulations is −5 mV.

4.2.2 Switching Delay Variation

The switching time of a ferromagnet is calculated in [111] using the small cone-angle approximation

$$\tau_{s,\omega} = \tau_0 \frac{ln(\pi/\theta_0)}{\chi - 1}, \tag{4.1}$$

where τ_0 is a fitting parameter, θ_0 is the initial angle of the magnet, and χ is the ratio of the magnitude of injected spin current to the critical spin current required for the switching of the magnetization of the output ferromagent. Based on this equation, if the value of injected spin current increases, the switching delay decreases. However, as shown in [101], the channel in this device can be approximated as an RC network; hence, the injected spin current and the value of supply voltage are directly correlated. Therefore, the switching delay is inversely proportional to the value of supply voltage. This result is shown in Figure 4.3. The device parameters used for these simulations are shown in Appendix B.

4.2.3 Impact of Thermal Noise

The thermal motion of electrons inside the ferromagents, is the main cause of thermal noise. The amount of noise is correlated to the temperature of magnets and can directly affect the steady-state precession angel θ_0. Based on the derivations in [110]

$$< \theta_0^2 >= \frac{K_b T}{E_b}. \tag{4.2}$$

In this equation, E_b is the barrier energy and T represents the temperature. This thermal effect acts as the main source of noise which can impact the output

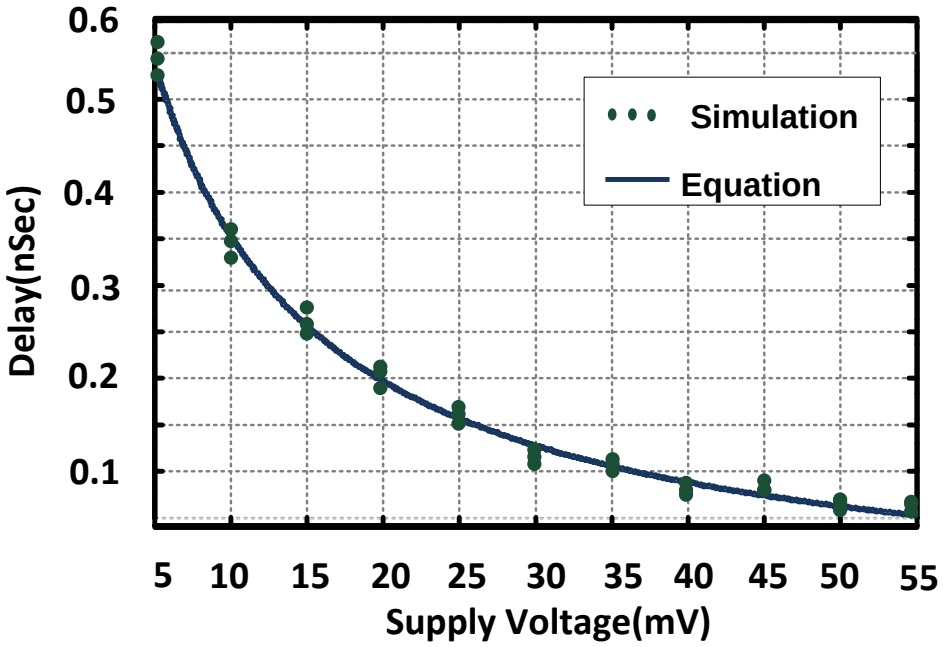


Figure 4.3: Switching delay variation versus the supply voltage. Each point is simulated 3 times to verify the results[104]

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magnetization. In our simulations, θ_0 can differ 5% to 10% from the analytic solution based on different parameters.

4.3 Pattern Recognition Scheme

Similar to any recognition system, in this work we consider two major phases for the operation. The first phase is the "learning" phase where the desired pattern is stored in memory. In "detection" phase, the circuit identifies the similarity of an input data and the stored pattern with respect to the decision making criteria. In the learning phase, the circuit can receive a single image or a training set. The training set includes multiple training images from different users.

In this section, we propose a new technique using all-spin logic devices and establish a fully spin-based operation. By illustrating several examples, we verify the performance for various image sizes.

4.3.1 Mainly Similar Images

We first provide the mathematical definition of mainly similarity and then show how this can help the training of the circuit. In our simulations, all the images are binary-valued matrices with 0 and 1 representing white and black pixels, respectively. In our circuit, we assume that binary "0" logic corresponds to magnetization orientation in $-X$ direction and binary "1" logic corresponds to magnetization orientation in $+X$ direction.

For a given pair of binary vectors x and y with equal length L, the *Hamming distance* [103] is defined as

$$d(x, y) = \sum_{i=1}^{L} 1 - \delta_{x_i y_i},$$

where x_i and y_i denote the i^{th} components of x and y respectively and δ is the kronecker delta. Subsequently, we can exploit this quantity as a measure of similarity between two images.

Definition 1 *Two binary images B and $B' \subset \{0,1\}^{m\times n}$ are called mainly similar if the majority of pixels across every two rows are identical. More specifically,*

$$\forall k \in \{1, \cdots, m\}: \qquad d(B_{k,:}, B'_{k,:}) < \lfloor \frac{n}{2} \rfloor, \tag{4.3}$$

where $B_{k,:}$ denotes the k^{th} row of B and $\lfloor a \rfloor$ represents the floor operation on a (i.e., the largest integer not greater than a).

By this comparison, we ensure that the two images have almost similar pixels along the corresponding rows. For the purpose of this paper, we considered the comparison along the rows, although a column-wise comparison could be established with no loss of generality. As illustrated in Figure 4.4, being mainly similar along the rows, does not imply being similar along the columns.

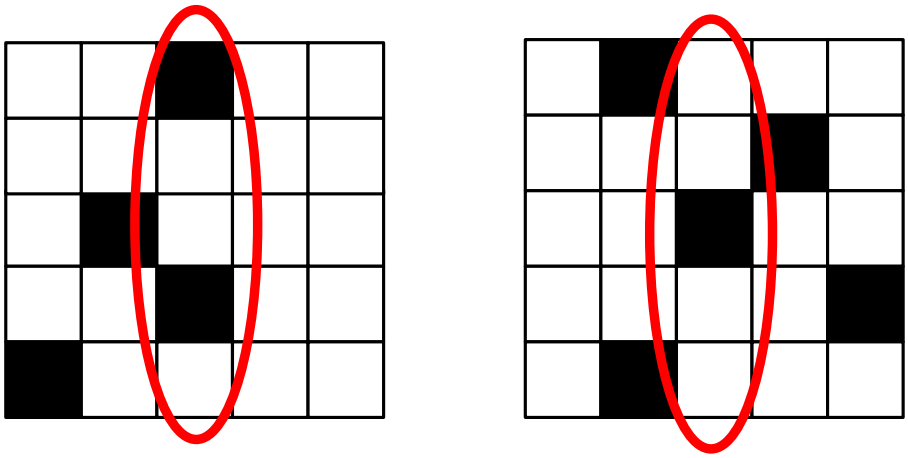


Figure 4.4: The two images are mainly similar (along the rows), however, the Hamming distance between the third columns is 3 which does not imply a similarity along the columns

4.3.2 Majority Training and Decision Making

In the learning phase, we train the circuit by providing a number of mainly similar images. In reality, these images could be different representations of a target image (say a character or a certain binary pattern). We build up a representative of the given similar images by constructing a so-called *mean image*.

Definition 2 *For a set of P binary images* $B_1, B_2, \cdots, B_P \subset \{0,1\}^{m\times n}$*, the corresponding mean image denoted as* $\bar{B}$ *is a binary image with entries*

$$\bar{B}(i,j) = nint(\frac{1}{P}\sum_{k=1}^{P} B_k(i,j)). \tag{4.4}$$

In this equation, *nint* denotes the nearest integer function. In our circuit, the mean image represents the desired pattern by the users and is utilized as a reference. Since this matrix is constructed using all-spin majority gates, the number of training images, P, is considered to be odd and upper bounded by the maximum number of inputs to a majority gate as discussed in subsection 4.2.1.

After the training data is stored and the mean image is constructed, we make a row-wise comparison between the input and the mean image. As we will see in the next section, depending on the initial value of output magnetization, the non-Boolean row decision maker can return the total count of matches or mismatches between the compared rows of input image and the mean image.

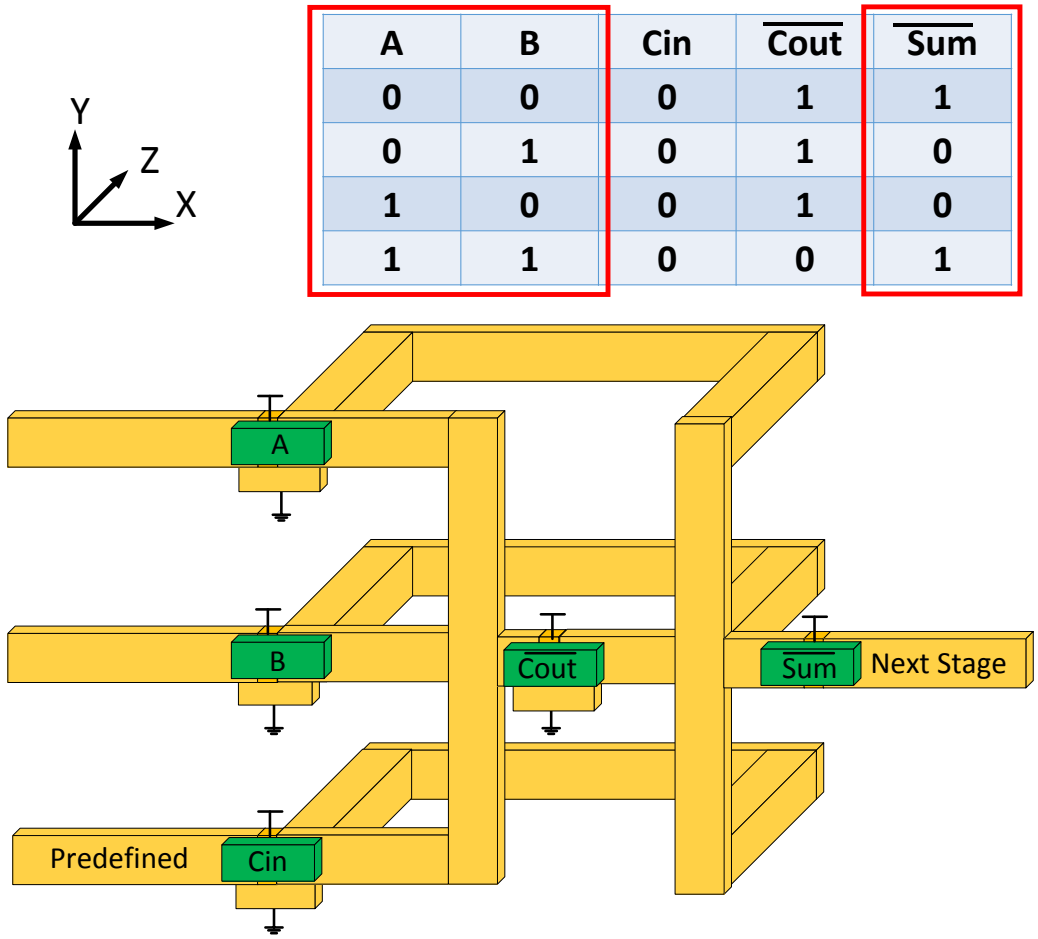
4.4 Proposed Structure and Design Considerations

Based on the pattern recognition scheme shown in Section III, we study two different implementations of the circuit. By comparing the performances of the two different versions of the *single pixel comparator* unit, we choose the one with more capabilities, at the expense of slightly more power consumption and occupied area. In the single pixel comparator, the circuit receives the training pixels from P different users and the mean image is constructed, subsequently. The value of the mean pixel is then compared with the corresponding value in the

input image and the steady state magnetization of *Pixel* magnet stores this information. The two versions of this unit both operate based on the idea of training the circuit with a set of mainly similar images and comparison of the single pixels from the input image with their correspondence in the mean image. With respect to the required operations, the single pixel comparator, needs a memory to store the training data, a logic comparator and a circuit to construct the mean pixel. As previously mentioned, the mean pixel can be constructed by an all-spin majority gate; however, for the memory and the comparator, we will propose a new circuit in the following subsection.

4.4.1 Memory+Logic Comparator

1-bit full adder structures with a total number of 5 nanomagnets have been designed in [104] and [105]. By proper setting of the circuit in [104], we use it as an area and power efficinet comparator (XNOR) block as shown in Figure 4.5. The two inputs to this block (A and B) are coming from distinct sources. One of the inputs comes from the input image synchronized with the control voltage and the other input is given to the circuit during the learning phase. Compared to a CMOS counterpart, this structure exhibits very important advantages. First, it requires 5 magnets whereas the CMOS version requires at least 8 transistors for XNOR implementation. Second, this circuit has the capability of storing the training information without extra static power consumption, whereas in CMOS, excess power is consumed to store this data [93]. Taking advantage of the non-volatile operation in ASL devices, the input magnets of this circuit can store the binary data and later the stored information is used to determine the



A	B	Cin	$\overline{\text{Cout}}$	$\overline{\text{Sum}}$
0	0	0	1	1
0	1	0	1	0
1	0	0	1	0
1	1	0	0	1

Figure 4.5: 1-bit full adder used as XNOR[104]. In the 2D implementation of this work, X and Y wires are in-plane metal wires and connections along the Z axis are vias.

magnetization direction of the next stages. Figure 4.6 shows the simulated output waveform (*sūm* magnet) of the XNOR block for different scenarios of input magnetization. As it is important to consider the breakdown current effects, we choose the 5mV supply voltage in our simulations. This is to ensure that the current density is safely below the breakdown value. It is noteworthy that for channels with higher breakdown current densities, higher voltages can be applied and the operation speed increases. The control voltage is applied on the magnets at $t = 0$.

The total power consumption of the XNOR gate is $11\mu W$ and the estimated area is less than $0.3\mu m^2$. As we apply a control voltage on the XNOR gate, the output magnetization remains in $-X$ orientation (initial condition of magnetization in this simulation) if the pixel values are different. In case of having similar inputs to this gate, the output magnetization switches to $+X$ direction as shown in Figure 4.6. We have to clarify that the initial condition of output magnet does not change the final magnetization orientation.

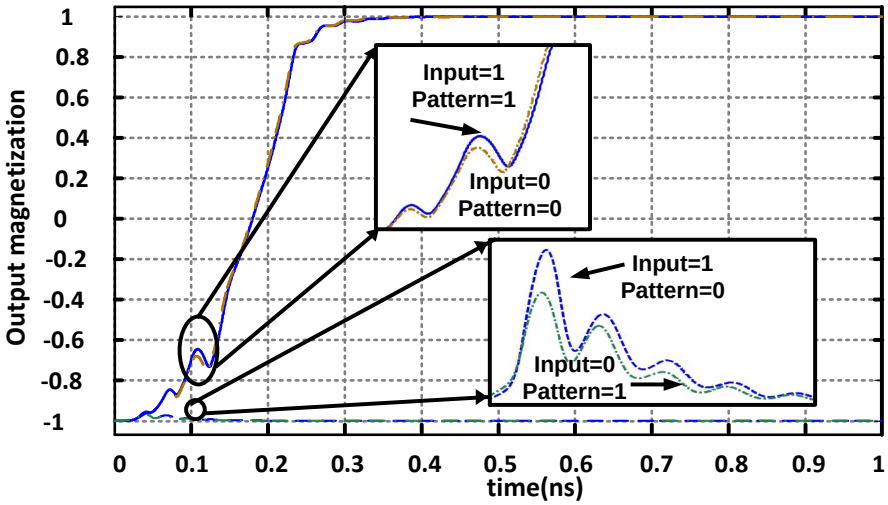


Figure 4.6: Simulated output waveforms of XNOR gate

4.4.2 Construction of the mean pixel

As a reliable and simple way to extract the information from the training set, we construct the mean image as discussed in Section III. The ASL majority gate with the schematic shown in Figure 4.2(b), provides a low power and efficient implementation of the mean image. The inputs to this majority gate, come from P different users. In addition, the images that system receives during the learn-

ing phase are constrained to be mainly similar along the rows. By applying the control voltage on the magnets of this gate, the output magnetization either switches to other value or remains in the same magnetization orientation. If the applied control voltage is negative, the output final magnetization orientation is the majority of the input magnetizations. In the case of positive control voltage, the output magnetization settles to the complementary majority value of the input magnetizations. For this system, since we apply unified positive voltages, the majority gates settle to the complementary majority value. In order to extract more information from the majority gates operation in this circuit, we assume a unified value of initial magnetization orientation on the output magnets of each stage of majority gates. This enables us to recognize the total count of matches or mismatches between the input magnetizations to each majority gate, as we will discuss later. The total power consumption of each majority gate in this circuit is $3.75\mu W$ and the corresponding estimated area is less than $0.2\ \mu m^2$.

4.4.3 Single Pixel Comparator

By having the required blocks, we propose the two different versions of the single pixel comparator.

Standard implementation

The schematic of this implementation and the table with the detailed operation are shown in Figure 4.7. This circuit operates in the same order discussed in

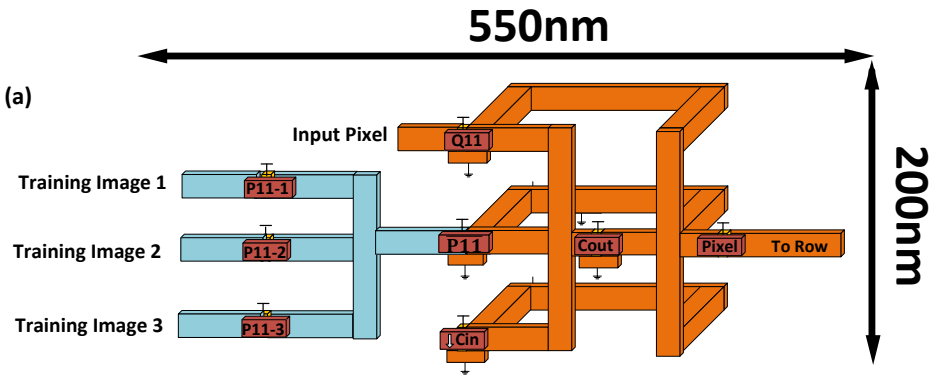
Section III. The first stage of the circuit is a majority gate with inputs coming from the P users in the learning phase. The output of this majority gate settles to the corresponding mean pixel value. The output of this gate is connected to a comparator circuit which has the other input coming from the input image. The connection is through a short metallic interconnect to minimize the delay. When the learning phase is over and the detection phase starts, by applying the control voltage across the magnets of the comparator circuit, the "Pixel" magnet settles to the comparison value of the mean pixel and the input pixel. It is noteworthy that the input pixel can be applied on magnet Q_{ij} after the $\bar{P_{ij}}$ magnetization settles to the mean pixel; hence, no extra memory circuit is required to store the value of $\bar{P_{ij}}$.

Comparator-First implementation

In this version, there are the same number of comparator circuits as the total number of training images at the input side. The comparators have the input image pixel, Q_{ij} in common and differ in their other input which comes from their corresponding training image. The output magnets of the comparators are connected to the "Pixel" magnet through metallic interconnects in a majority gate configuration. During the learning phase, the pattern pixels are stored in the corresponding input magnets. By applying the control voltage on the magnets of the circuit, the detection phase starts and the "Pixel" magnetization settles to the comparison value of the mean pixel and the input pixel. The schematic of the circuit and the detailed operation table are shown in Figure4.8.

As it can be verified by comparing the last columns of Figure4.7(b) and Figure4.8(b), the "Pixel" steady state value is identical in the two versions. To

(a)



(b)

Input Pixel	Pattern 1	Pattern 2	Pattern 3	Majority Initial Value	Majority Switching	Mean Pixel	Output Final Value
0	0	0	0	1	NO	0	0
0	0	0	1	1	NO	0	0
0	0	1	0	1	NO	0	0
0	0	1	1	1	YES	1	1
0	1	0	0	1	NO	0	0
0	1	0	1	1	YES	1	1
0	1	1	0	1	YES	1	1
0	1	1	1	1	YES	1	1
1	0	0	0	1	NO	0	1
1	0	0	1	1	NO	0	1
1	0	1	0	1	NO	0	1
1	0	1	1	1	YES	1	0
1	1	0	0	1	NO	0	1
1	1	0	1	1	YES	1	0
1	1	1	0	1	YES	1	0
1	1	1	1	1	YES	1	0

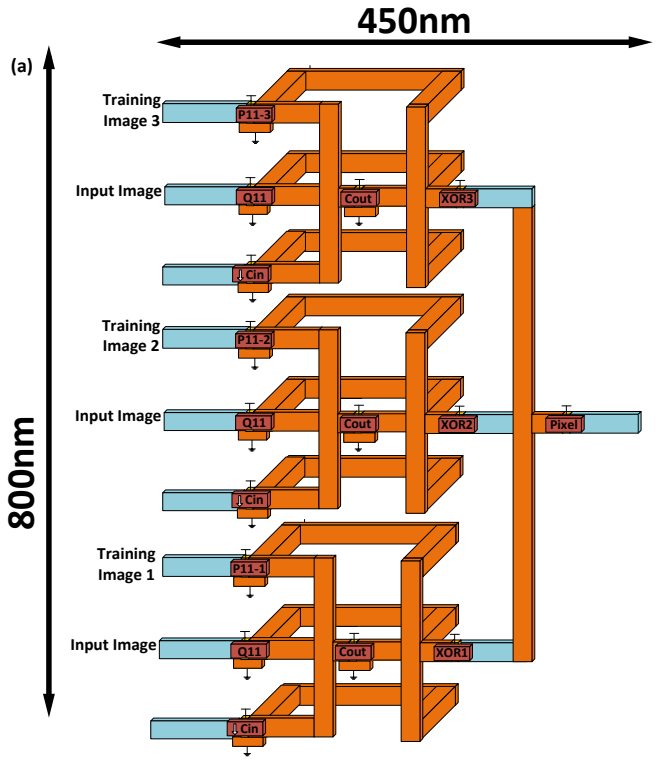
Figure 4.7: (a) Standard single pixel detector schematic. (b) The truth table with the detailed operation of the circuit.

verify the identical output result from the two different versions of the implementation in a more general case, we have to prove that the majority operation and the comparison (XOR/XNOR) operation are interchangeable, i.e.,

Proposition 1 *Given $x, y_1, y_2, \cdots, y_P$ as binary variables and P as an odd integer number,*

$$x \oplus nint(\frac{1}{P}\sum_{k=1}^{P} y_k) = nint(\frac{1}{P}\sum_{k=1}^{P}(x \oplus y_k)), \tag{4.5}$$

where $\oplus$ denotes the XOR operation. The mathematical proof of this proposition is shown in Appendix A.



(b)

Input Pixel	Pattern 1	Pattern 2	Pattern 3	Output Initial Value	Output Switching	Output Final Value
0	0	0	0	1	YES	0
0	0	0	1	1	YES	0
0	0	1	0	1	YES	0
0	0	1	1	1	NO	1
0	1	0	0	1	YES	0
0	1	0	1	1	NO	1
0	1	1	0	1	NO	1
0	1	1	1	1	NO	1
1	0	0	0	1	NO	1
1	0	0	1	1	NO	1
1	0	1	0	1	NO	1
1	0	1	1	1	YES	0
1	1	0	0	1	NO	1
1	1	0	1	1	YES	0
1	1	1	0	1	YES	0
1	1	1	1	1	YES	0

Figure 4.8: (a) Comparator-first pixel detector schematic. (b) The truth table with the detailed operation of the circuit.

Although the standard implementation has slightly lower power consumption (Less number of devices) and a smaller area, we select the comparator-first design as the unit cell of this circuit. This is due to the fact that the output mag-

netization transient of this circuit provides more information on the similarity of the training pixels and the input pixel. Based on Fig **??**(b) and Figure4.8(b), the final value of output magnetizations, in the two cases are identical. However, the Comparator-first output magnetizations is coming from a majority gate and switches when the majority of pattern pixels have the same value of the input pixel. If the majority gate at the output of Comparator-first circuit has a low fan-in (e.g., $\leq$ 5), the switching transient behavior will be less sensitive to the accumulated thermal noise and the information on the number of training pixels with identical values will be provided. On the other hand, in the standard implementation, the output magnetization is from the XNOR circuit and conveys no information on the number of similar pattern pixels. Based on Fig **??**(b), the output magnetization transient will not add information on the number of training pixels with identical values. This is particularly important when the user in the detection phase tracks the total count of pattern pixels with the similar value.

4.4.4 Non-Boolean Row Decision-Maker

The last stage of the proposed circuit uses the interesting feature of the ASL majority gate as a means to quickly decide about the mainly similarity of the input image and the mean image, along the rows. The inputs to this majority gate is from the "Pixel" magnets of the pixels along the same row of the image. The connection is through short interconnects to minimize the delay. As mentioned before, the spin torque transferred from the input magnet to the output magnet in the ASL majority gate, is determined by the magnetization of the input devices. As the number of devices with similar magnetization orientations in-

creases, the transferred spin torque increases; hence, the output magnetization switching becomes faster according to (3). By proper selection of the control voltage timing and also the dimensions of the nanomagnets and metallic interconnects in this gate, a reliable decision-making based on the transient behavior of output magnetization is achieved. This final majority gate is sensitive to the uncorrelated thermal noise of input magnets; hence, an intentional low fan-in number (≤ 5) has to be selected. In our simulations, 3 magnets from the previous pixel stages are connected to this gate and as it will be shown in simulation results, a reliable decision-making is achieved.

The complete circuit for the full image comparison consists of two stages. The unit pixel comparator and the row majority gate. The structure consisting of the comparator-first circuits and the Row majority gates is called the "Smart Detector Cell". This naming convention, helps the discussion of operation in the next section. We call these detector cells smart because they can perform multiple tasks of "storage", "Boolean Computation" and "non-Boolean decision-making" in a time-efficient manner. The schematic of this circuit is shown in Figure 4.9. The total power consumption of this circuit is 115 μW and the occupied area is less than 0.5 μm^2.

We have to mention that in our simulations, we have taken into account the effect of magnetization switching. The ASL device acts like a resistive network and the power consumption will not change with time. In these devices, the current passes through only one magnet and therefore does not change with time and the magnet switching of the input side, will influence the switching delay of the last magnet. In addition, we consider the worst case delay which

takes into account the switching delay from the input magnet of the first device to the output magnet of the last device as well as the transport delay within the metallic interconnects. For DC power consumption estimations, we have performed DC and transient simulations and the results are consistent. It is noteworthy that the low operational voltage of the circuit will lead to a low power consumption.

In a real implementation of this work, read/write circuits are added to fully realize the circuit. However, this paper focuses on the processing circuit without concerns regarding the feeding and extraction of the input and output data. In order to feed the input data, spin polarized currents are used to initialize the magnetization of input magnets based on the training images, similar to [95]. On the other hand, the number of write units is equal to the number of pixels, while there is one output, which translates to small overhead. The decision data is in form of time delay and can be stored on a capacitor, where the delay impacts the amount of the stored charge. The other possibility to extract he output data will be using MTJ devices, as mentioned in [114].

4.5 Simulation Results

In this section, we provide two different examples to show the reliable performance of smart detector cells.

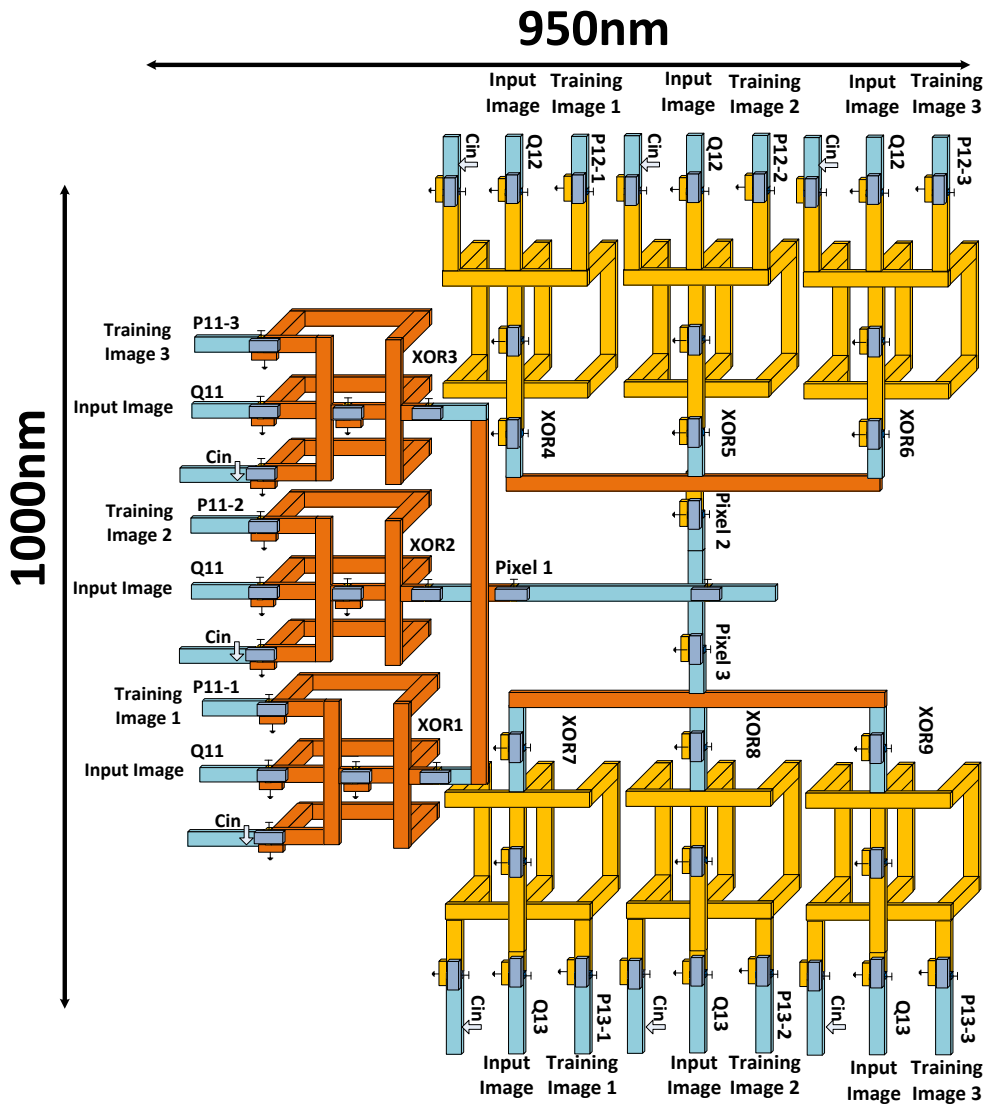


Figure 4.9: Structure of the unit smart detector cell

4.5.1 Non-Boolean Hamming Distance Identifier of 3×3 Pixel Pattern and Input Image

In this example, we only have one training image and one input image. To compare the similarity of these two images, we need 9 XNOR gates to identify the similarity of corresponding pixels in the two images and 3 majority gates

with Fan-in of 3 to decide on the similarity of the corresponding rows. It is also obvious that the mean image in this case will be the same pattern image. The smart detector cell in Figure4.9, has 3 comparator-first circuits and a *Row* majority gate. The mainly similarity of the rows can be determined by the Pixel majority gates. The last majority gate in this case, settles to $+X$ magnetization if at least 2 rows are mainly similar. The initial magnetizations of the comparators and the majority gate outputs are set to 1. Figure 4.10 shows the two images as well as the transient magnetization for various magnets. The Pixel waveforms overlap in some cases and that is why we are showing only 3 pixels in this Figure. As expected, the comparator outputs switch for P_{21} and P_{22} pixels since the values in the input image and the pattern image are different. For the rest of pixels, the comparator output is $+X$ magnetization and will not switch. Subsequently, row 1 and row 3 both exhibit perfect similarity and the output of the corresponding majority gates switch within the shortest time. On the other hand, row 2 exhibits a mismatch and therefore can not switch to $-X$ magnetization orientation. The control voltage of 5 mV is applied on all the magnets at $t = 0$ and the circuit compares the two images in less than 0.6 ns. Compared to CMOS circuits, this exhibits a much lower operational voltage and decision time.

4.5.2 Non-Boolean Similarity Comparison of a 9×9 Pixel Image and a Set of 3 Pattern Images

In order to incorporate the smart detector cells for larger images, we need an accurate design of the cells. Here, we develop a circuit for training with 9×9

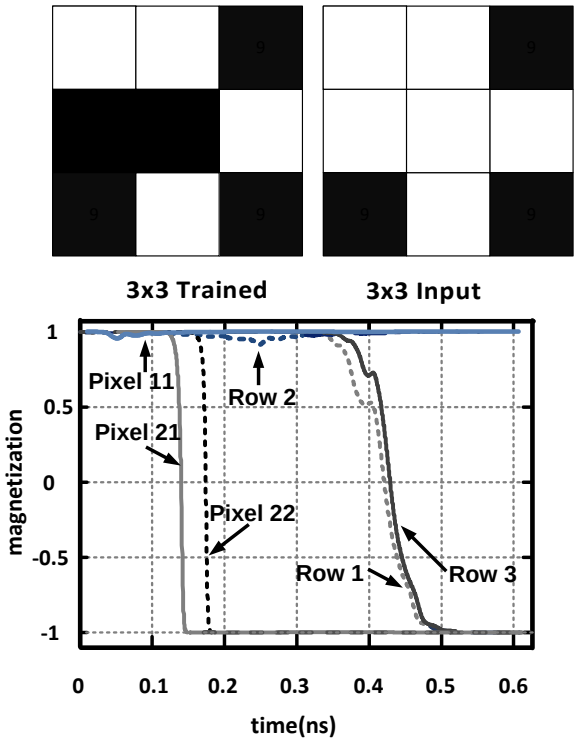


Figure 4.10: Using a single smart detector cell, we can compare these 3×3 pixel images. The waveforms of the comparators and majority gates (bottom).

pixel images and perform a non-Boolean comparison between the constructed mean image and the 9×9 pixel input image. In this simulation, 3 different users write the word "Spin" by their own choice of pixels. The 3 pattern images are shown in Figure 4.11.

In the detection phase, a new user of the circuit, chooses an arbitrary image of interest as the input. As an example in this simulation, the user chooses the word "swim" as shown in Figure4.12 (left). The circuit should compare this image and the mean image constructed from the training set.

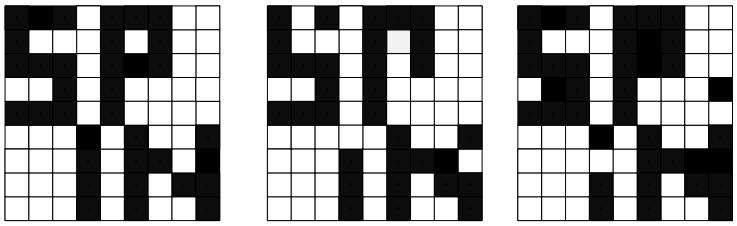


Figure 4.11: Training set for the 9×9 pixel images

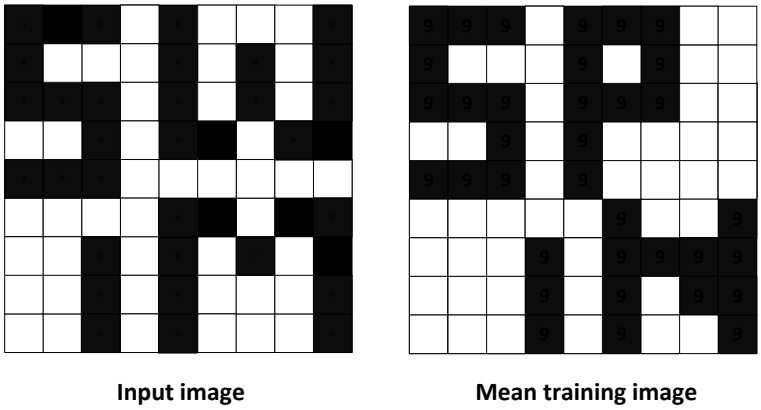


Figure 4.12: The input image (left) and the representation of the mean image (right). The mean image is not a direct output of the circuit.

The mean image of the training set is also shown in Figure4.12 (right). One particular advantage of constructing the mean image can be discussed here. As it can be seen in Figure 4.12, those pixels which are mistakenly valued by a single user (e.g., P_{26} and P_{49}) in the learning phase, are automatically corrected when the mean image is constructed. This is specifically useful, when the users during the learning phase, train the system with multiple versions of an image to make sure that the mean image represents their desired pattern. The mistaken values could be due to any source of error or distortion. In an ideal case where the thermal noise effect can be ignored, by simply changing the fan-in

of different stages in the smart detector cell, the circuit can compare these two large images. However, in our simulations, as we model the thermal noise accurately, the fan-in considerations mentioned before, are particularly important. Based on these considerations, we break these 9×9 images into smaller 3×3 sub-images, where a single smart detector cell unit can be used for the comparison. The 9 smart detector cells can operate in parallel and the circuit configuration can be determined by the user. By this breakdown, we can also achieve more information on the pixels as we can check the mainly similarity for smaller blocks of the original image. The breakdowns of the mean image (squares on the right) and the input image (squares on the left) are shown in 3×3 partitions in Figure **??**.

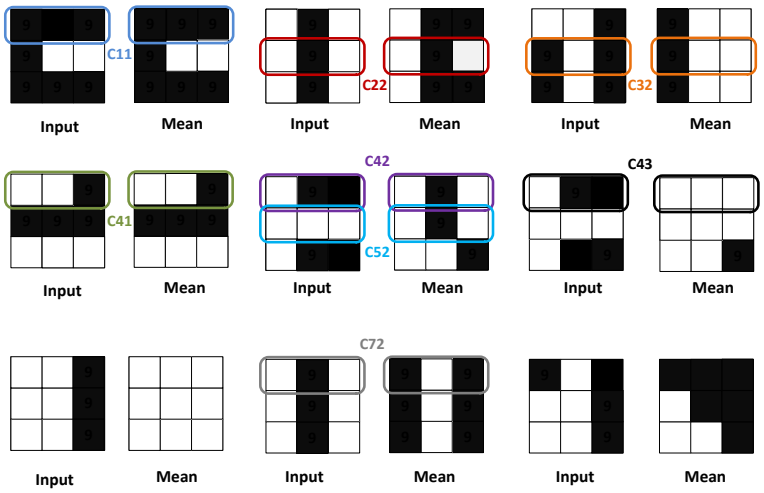


Figure 4.13: Due to fan-in considerations, the circuit is consisted of 9 smart detector cells. The corresponding breakdowns of the mean image and the input image are shown here .

In order to distinguish the different rows of smaller blocks, we use the notation of C_{ij} clusters, which represents the elements of the i^{th} row from column $3j-2$ to column $3j$. The magnetization waveforms shown in Figure 4.14 and

Figure4.15 separately show the output magnetizations of smart detector cells for various clusters. The unified initial condition of the output magnet in this simulation is $-X$ magnetization orientation. In Figure 4.14, the switching delay of output magnetizations for the clusters with perfect match (C_{11}, C_{22} and C_{41}) and those with 1 mismatch (C_{52}, C_{42} and C_{32}) can be easily distinguished. This phenomenon was previously described as the unique feature of ASL majority gates and helps the users to identify the number of mismatches along different rows. At the same time, the output magnetization of the clusters with the same level of similarity, are very close in time domain which makes this non-Boolean decision-making a reliable metric. On the other hand, in Figure 4.15,

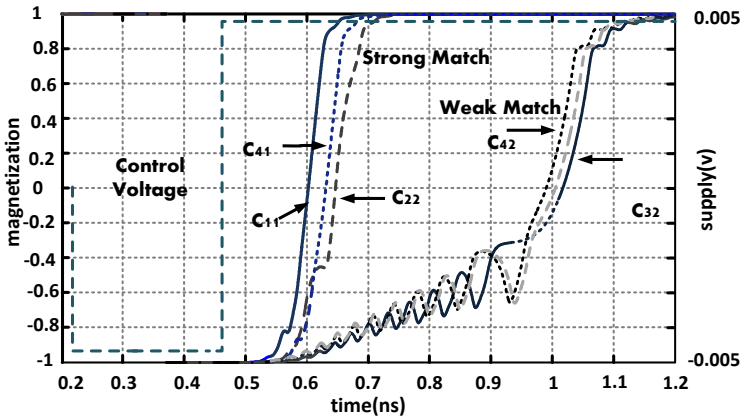


Figure 4.14: The switching delay of output magnetization in last stage represents the similarity of input data and pattern data.

the output magnetization can not switch for clusters with mismatches (C_{43} and C_{72}) and as it can be seen, the level of precession for different mismatch levels is not the same. This is due to the different amount of spin torques provided in these two cases. If the user has a very high resolution study on the output magnetization, this can help to identify the number of mismatches; however, the switching transient is a more reliable metric and the same information can

be extracted by repeating the simulation with the output magnet initial condition set to $+X$ magnetization.

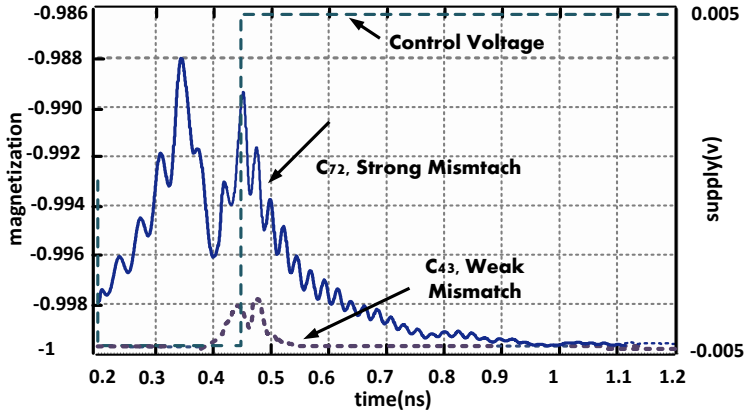


Figure 4.15: Since these clusters represent mismatch, they can not switch and the initial magnetization does not change. Note that the y-axis is showing from -1.002 to -0.998 in contrast with Figure 4.14 in which the y axis is from -1 to 1.

As it can be seen in all the simulation results, this circuit can make a decision in almost 1000 ps for a 9×9 pixel image, whereas in CMOS, this decision time, can not be less than few nanoseconds. For a detailed comparison between the two technologies, in table 1, the performance of this circuit and two existing CMOS circuits are compared.

4.6 Conclusion

We have presented a novel non-Boolean image recognition circuit based on all-spin logic devices. The introduced circuit can perform all the phases of a non-Boolean pattern recognition for binary images. Taking advantage of the

Table 4.1: Performance Comparison with existing CMOS systems

Reference	**[90]**	**[95]**	**This Work**
Decision time	30ns	N.A.	1 ns
Image Size	32×32	86 neurons	9×9
DC Power	N.A.	$2.2mW$	990 uW
Area	N.A.	$0.018mm^2$	$< 1\mu m^2$
Technology	CMOS	Spin-CMOS	All-spin

non-volatility of ASL devices, the learning phase operation is performed incorporating no additional memory devices. By introducing the mainly similarity scheme, two different implementations of the circuit are proposed. As verified by simulation results, this circuit can recognize various sizes of binary image patterns faster than existing CMOS counterparts and consumes less power with an operational voltage of 5mV. Since the comparisons in this circuit are based on ASL majority gates, the computational complexity of the operation is also less compared to existing circuits. The proposed circuit has applications in fast and low power image recognition for security, medical imaging, and sensing.

4.7 Proof of proposition 1

In this appendix, we mathematically verify (7). Since all the variables are binary-valued,

$$0 \leq \frac{1}{P} \sum_{k=1}^{P} y_k \leq 1.$$

The *nint* operation results in 0, when

$$\sum_{k=1}^{P} y_k < \frac{P}{2}, \tag{4.6}$$

otherwise it results in 1. Therefore, there are 4 different possibilities for the variables, as shown in table II. In order to simplify the notations, we also define,

$$z_k = x \oplus y_k \qquad \forall k \in \{1, \cdots, P\}. \tag{4.7}$$

Table 4.2: Possibilities of $x, y_1, \cdots, y_P$

x	$\sum_{k=1}^{P} y_k$	$nint(\frac{1}{P} \sum_{k=1}^{P} y_k)$	$x \oplus nint(\frac{1}{P} \sum_{k=1}^{P} y_k)$
0	$< \frac{P}{2}$	0	0
0	$> \frac{P}{2}$	1	1
1	$< \frac{P}{2}$	0	1
1	$> \frac{P}{2}$	1	0

Here, we verify (7) for the first row of table II. Using the same method for the other 3 rows, the proposition can be completely proved.

If $\sum_{k=1}^{P} y_k < \frac{P}{2}$, fewer than $\frac{P}{2}$ of y_k's are 1. Given $x = 0$, this means that fewer

than $\frac{P}{2}$ of z_k's are 1 and the rest are zero, i.e.,

$$\sum_{k=1}^{P} z_k < \frac{P}{2}.$$

Similar to (8), by applying the nearest integer function,

$$nint(\frac{1}{P}\sum_{k=1}^{P} z_k) = 0.$$

4.8 Simulation Parameters

Size Effect Parameters[99]		
Side Wall specularity	P	0
Grain Boundary Reflectivity	R	0.2
Interface Parameters(Co/Cu)[109]		
Majority Spin conductance	$G_{\uparrow}$	0.375 $1/\Omega$
Minority Spin conductance	$G_{\downarrow}$	0.125 $1/\Omega$
Real Spin-Mixing Conductance	$\mathrm{Re}G_{\uparrow\downarrow}$	$3.43751/\Omega$
Imaginary Spin-Mixing Conductance	$\mathrm{Im}G_{\uparrow\downarrow}$	9.37×10^{-3} $1/\Omega$
Ferromagnet(Co)[112]		
Ferromagnet Length	L_x	75.00 nm
Ferromagnet Width	L_y	25.00 nm
Ferromagnet Height	L_z	3.00 nm
Gilbert Damping Coefficient	α	0.0021
Gyromagnetic Ratio	γ	1.76×10^{11} $1/\mathrm{sT}$
Saturation Magnetization	M_s	1.45×10^{6} A/m
Number of spins in magnet	N_s	1.34×10^{6} $1/\mathrm{V}$
Energy Density	K_u	$0.5\times10^{5} J/m^2$
Channel(Cu)[113]		
Channel Length	L_{int}	212.5 nm
Channel Width	W_{int}	50 nm
Thickness/Width aspect ratio	AR	2.0
Channel Thickness	H_{int}	100.0 nm
Cross section Area	A	5000 nm^2
Finite difference spacing	Δx	10.0 nm
Conductivity	σ	41.549 $1/\mu\Omega m^2$
Diffusion coefficient	D	0.014 m^2/s
Permeability	μ	0.003 m^2/Vs
Spin relaxation time	τ_s	10.939 ps

CHAPTER 5

A SIGE TERAHERTZ HETERODYNE IMAGING TRANSMITTER

5.1 Introduction

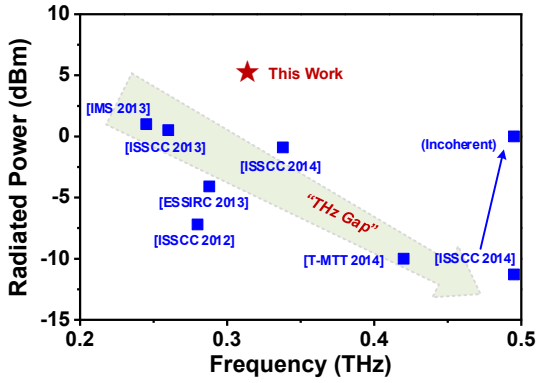
Electromagnetic radiations in the terahertz range has demonstrated great potential in the imaging applications for biomedicine, security and industrial quality control [115], due to its high spatial resolution (compared to millimeter wave) and non-ionizing natures (compared to X-ray). At present, the barrier to the wide application of this emerging sensing technology is mainly due to the difficulty of the high-power signal generation. Conventional THz sources include quantum-cascade laser (QCL)[116], photoconductive emitter [117], and vacuum electronics. However, these solutions have significant drawbacks, such as the high cost, large form factor and stringent operation conditions (e.g. cryogenic cooling for QCL), etc. Because of these, active THz imaging microsystems using integrated circuit technology is drawing increasing attentions . In particular, imagers based on CMOS and BiCMOS processes are expected to not only resolve the above problems, but also achieve an high systematic integration level [119][120]. This makes affordable and portable THz imaging equipment possible.

However, there are several technical barriers on the paths towards this goal. First, the radiated power of nowadays THz transmitters in silicon is still insufficient. This is mainly due to the limited speed and breakdown voltage of the silicon transistors. The first THz CMOS radiator source reported in 2008 only generates 20-nW power [121]. Ever since then, significant progress has been made with synergistic efforts in device, circuit and electromagnetism. In [122], 390-

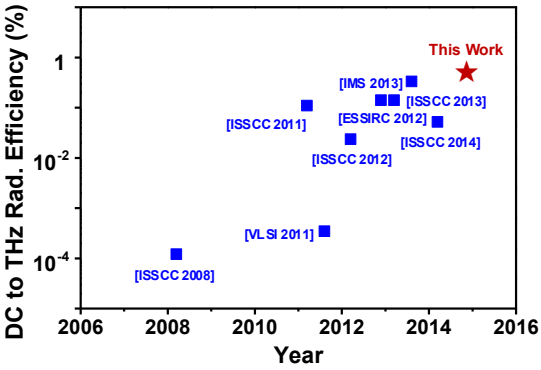
μW power is obtained in the 288-GHz radiator based on a triple-push oscillator topology. In [123], the 338-GHz phased array achieves 810-μW power. In [124], a self-feeding oscillator array generates 1.1-mW radiated power at 260 GHz. Besides these work in CMOS, radiation sources in BiCMOS processes also demonstrate great potential, thanks to the superior speed and breakdown voltage of the SiGe heterojunction bipolar transistor (HBT) [125].

To some extent, larger total radiated power can be obtained through the combination of an increasing number of array elements. By comparison, the DC to THz radiation efficiency is more relevant to the performance of the devices and basic circuit blocks. Such merit is also very important for energy and thermal limited portable systems. As Figure5.1(b) shows, within less a decade, the DC to THz radiation efficiency of silicon sources has increased by over three orders of magnitude. However, due to the approach of harmonic generation, the absolute efficiency level is still low. Previously reported highest DC to THz radiation efficiencies are 0.14% in CMOS [122][124] and 0.33% in SiGe BiCMOS [126].

The challenge of the on-chip active THz imaging system also resides in the receiver side. Due to the lack of power amplification for THz signals (f_{in}>f_{max}), focal-plane arrays in silicon rely on the direct passive detection using nonlinear devices, such as Schottky diode [119] and MOSFET [120]. This leads to poor sensitivity and further requires high-power generation from the transmitter. On the other hand, due to the Rayleigh diffraction limit [127] and the usage of resonant antenna coupling, the size of an imaging pixel at THz, especially at low-THz (~300 GHz) is large. It is therefore difficult to accommodate a large number of pixels on a single silicon die andmechanical scanning is commonly used.



(a)



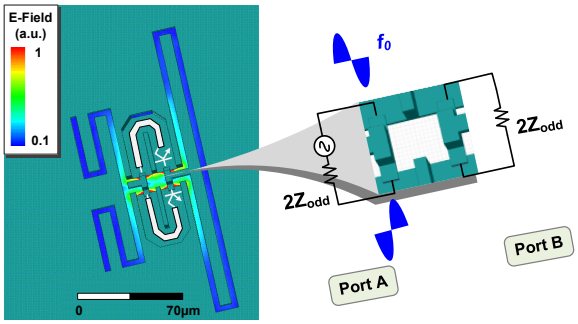
(b)

Figure 5.1: The performance of the state-of-the-art THz radiator sources in silicon: (a) the total radiated power at varying frequencies and (b) the achieved DC to THz radiation efficiency over the past few years.

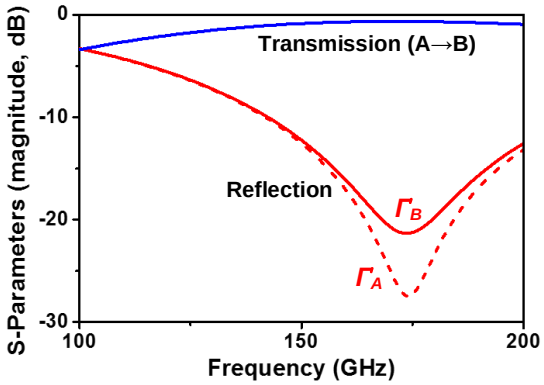
5.2 Design of a 320-GHz Transmitter

5.2.1 Simulation Results

The operations described above are verified in the full-wave electromagnetic simulations using HFSS [133]. First, the return-path gap structure is stimulated by a differential (odd-mode) signal. The two-port simulation set up is shown in



(a)



(b)

Figure 5.2: Full-wave electromagnetic simulation of the THz radiator: (a) odd-mode excitation/loading ports and the intensity distribution of the electrical field (b) S-parameters near the fundamental oscillation frequency of 160 GHz.

Figure 5.2(a)[1]. Figure 5.2(a) also presents the intensity distribution of the electrical field inside the slots of the structure at the fundamental oscillation frequency of 160 GHz. It can be seen that the odd-mode signal is able to propagate along the return-path gap, and transfer from the differential Port 1 to Port 2. Meanwhile, standing waves are formed inside the four folded RF-choke slots. The results of the S-parameter simulation are plotted in Figure 5.2(b). At 160 GHz, the insertion loss (S_{21}) of the structure is only 0.6 dB, which proves that the return-path gap is transparent to the differential oscillation signal.

[1]The self-feeding lines and the two transistors (in white) in Figure 5.2(a) and Figure 5.4(a) are only for the purpose of illustration. They are not included in the actual EM simulation structure.

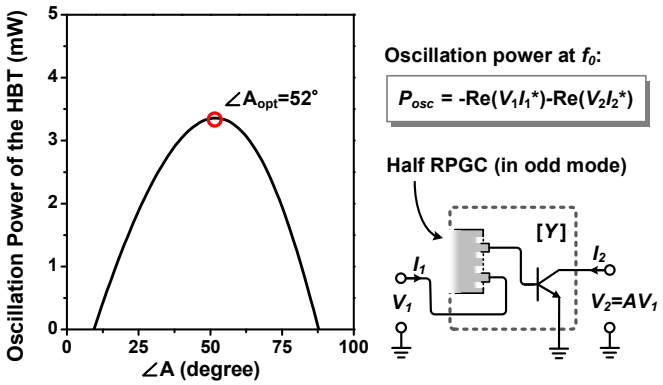
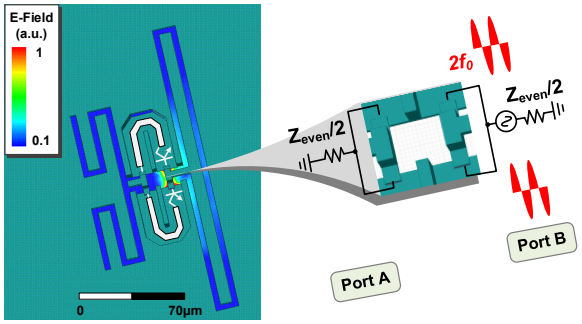


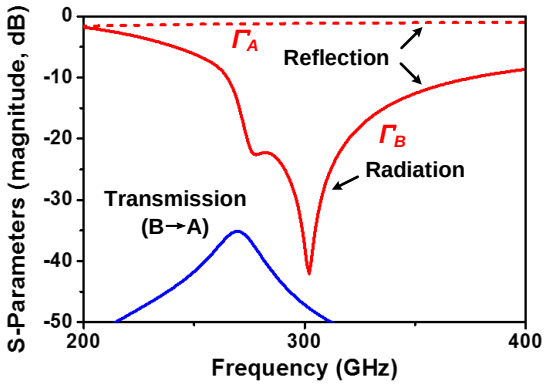
Figure 5.3: The two-port active network including a SiGe HBT and a series half-RPGC structure at the transistor base. Also shown is the simulated optimum phase of the complex voltage gain of such active network at 160 GHz.

Although the RPGC inserted in series with the transmission lines of the self-feeding oscillator pair does not add much loss, the induced phase shift cannot be ignored. Therefore, the HBT and one half of the RPGC (in odd-mode operation) can be considered to be a new equivalent "transistor" (Figure 5.3). By simulating the Y-parameters of such combined network, we see that the optimum phase of the voltage gain is 52° (or -308°).

For the common- (even-) mode operation, the simulation set up is presented in Figure 5.4(a). The stimulus from Port B represents the in-phase 2^{nd}-harmonic signal generated at the two bases of the SiGe HBTs. At 320 GHz, the intensity distribution of the electrical field inside the slots is shown in Figure 5.4(a) too. It is evident that the injected signal is fully blocked by the return-path gap. Meanwhile, four standing waves inside the folded slots on the right are formed. As indicated in Figure 5.4(b), the simulated isolation between the two sides of the return-path gap is better than -30 dB, meaning that the structure is opaque to the even-mode signal. Please also note that the small reflection coefficient at Port B (Γ_B) means that the 2^{nd}-harmonic signal is fully absorbed by the struc-



(a)



(b)

Figure 5.4: Full-wave electromagnetic simulation of the THz radiator: (a) even-mode excitation/loading ports and the intensity distribution of the electrical field (b) S-parameters near the 2^{nd}-harmonic frequency of 320 GHz.

ture. In fact, the signal is turned into a downward-propagating radiation wave inside the silicon; and the simulated radiation pattern is shown in Figure 5.5. The directivity in the perpendicular direction is 5.6 dBi. To reduce the excitation of the substrate-mode wave inside the silicon substrate (250-μm thick), a backside hemispheric silicon lens is assumed in the simulation (modeled as a semi-infinite silicon boundary condition beneath the chip substrate) [136]. The simulated radiation efficiency, including ~30% power reflection at the silicon-to-air interface [124], is as high as ~50%. The additional loss is due to the finite substrate resistivity (~10 Ω·cm).

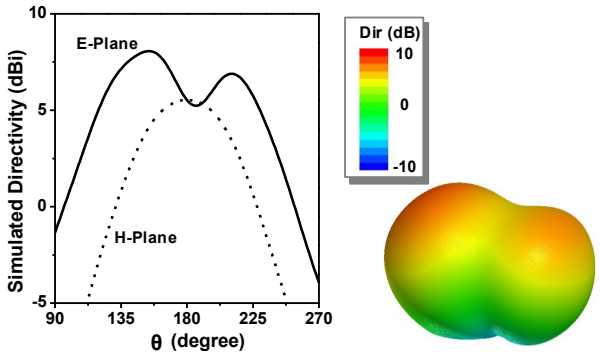


Figure 5.5: The simulated radiation pattern of the proposed 320-GHz radiator unit. A backside hemispheric silicon lens is assumed.

Lastly, from Figure 5.2(b) and Figure 5.4(b), it can be seen that the orthogonal behaviors of the proposed structure for odd and even mode signals have a very broad bandwidth. This makes the RPGC structure suitable for future implementations of wide-tuning source and broadband data transmitter.

The proposed RPGC-based THz radiator is integrated into a 4×4 array of a 320-GHz transmitter for heterodyne imaging system (shown in Figure 5.6). Compared to the incoherent fully-intensity-based detection (e.g. [119][120]) where the incident THz wave undergoes a self-mixing, in heterodyne detection it is mixed with an LO signal with much larger power. The output response, as well as the imaging sensitivity, are therefore greatly enhanced [134]. Meanwhile, the sinusoidal output of the heterodyne detector also preserves the phase of the incident THz wave at each pixel. This enables electronic beam scanning in a multi-pixel configuration, which could potentially eliminate the needs for the mechanical scanning in conventional THz imaging systems (discussed in Section 5.1). To perform heterodyne detection, it is critical to lock the phase of the RF signal in the transmitter and the LO signal in the receiver. To achieve this goal, in Figure 5.6 the 16-element radiator array is phase-locked by a fully-integrated PLL through injection locking at 160 GHz. The phase of the radi-

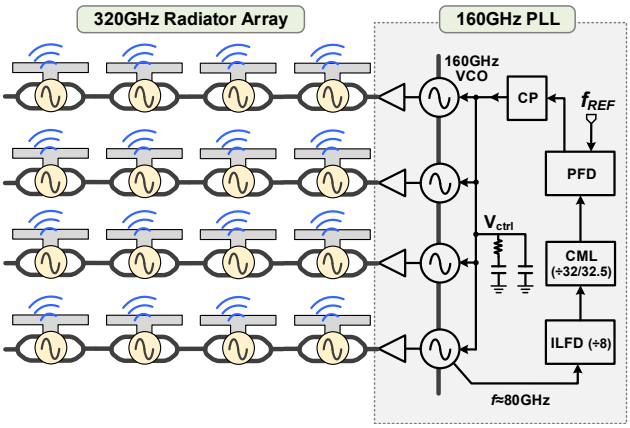
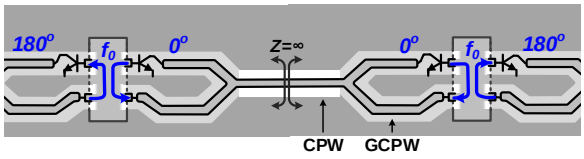
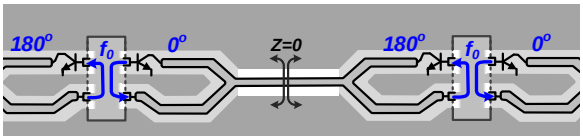


Figure 5.6: The architecture of the 320-GHz transmitter with a fully-integrated phase-locking loop.



(a)



(b)

Figure 5.7: The mutual coupling between adjacent radiators: (a) in-phase coupling mode (supported) (b) out-of-phase coupling mode (unsupported).

ated wave at 320 GHz is then locked to an externally applied reference clock at ~310 MHz. Next, some critical design details of the transmitter are given.

5.2.2 Coupled Radiator Array

Although the proposed return-path gap structure optimizes the generation efficiency of THz radiation, the absolute power level generated by each radia-

tor unit is still limited by the HBT size. Therefore the 16-element array is implemented for increasing the total radiated power. The power combining is through the constructive superposition of the radiated waves in the far field. Such quasi-optical power combining [135] is efficient, broadband, and highly scalable. The array is partitioned into four rows, in which elements are passively coupled. The mutual coupling between radiators is through a CPW transmission line tapping on the self-feeding lines of the radiators (shown in Figure 5.7). By symmetry, there are in-phase and out-of-phase coupling modes in the steady state[2]. In the in-phase coupling mode (Figure 5.7(a)), the boundary between two units is equivalent to an open termination, hence the added CPW lines behave as shunted capacitors. To minimize the impact of such capacitors, the signal path of the CPW lines is designed to be very narrow (W=3 μm) and far from the ground (D=6 μm). On the other hand, the out-of-phase mode (shown in Figure 5.7(b)) leads to a virtual ground at the connector of the coupling lines. It presents highly inductive suseptance in shunt with the self-feeding lines, which greatly reduces the oscillation power; this undesired mode is therefore naturally suppressed.

Due to the compactness of the proposed radiator design, the entire 16-radiator array, equipped with functions of fundamental oscillation, harmonic generation and on-chip radiation, only occupies an area of 0.9×0.9 mm^2. As a result, the achieved radiator density is ~4X higher than the prior arts [123][129]. The small radiator pitch also helps suppressing the side lobes of the combined beam. The simulated radiation pattern of the array is shown in Figure 5.8. The simulated peak directivity is 17.6 dBi.

[2]Any coupling phase between 0° and 180° leads to net power flow between units, and is therefore unstable. The mutual dragging and pulling eventually converges back to either in-phase/out-of-phase modes.

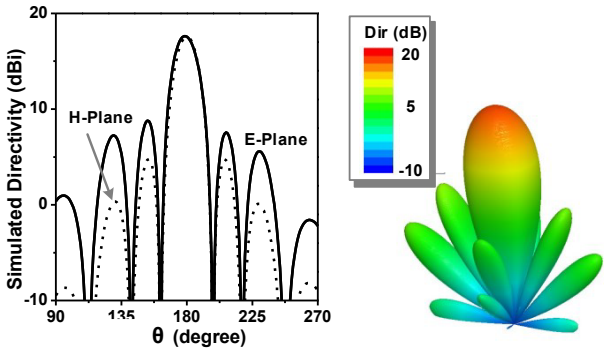


Figure 5.8: The simulated radiation pattern of the 320-GHz 4×4 radiator array. The pitch between the elements is 220 μm, and a back-side hemispheric silicon lens is assumed.

5.2.3 On-Chip Phase-Locked Loop

Shown in Figure 5.6, the on-chip PLL consists of 4 coupled VCOs, providing 160-GHz injection-locking signal to each radiator row. A divider chain samples the phase/frequency of the VCO linear array and then a global phase/frequency control signal V_{ctrl} is provided through a phase detector cascaded by a charge pump. Figure 5.9 presents the schematic of the VCO, including two output buffers at 80 GHz and 160 GHz. The VCO is based on a differential Colpitts oscillator topology, in which the resonance tank on one side is mainly formed by the transmission line stub TL_1, MOS varactor C_1 and the C_π of the HBT transistor Q_1. Compared to the cross-coupled topology, the advantage of the Colpitts oscillator is that the large, untunable C_π is in series with C_1; therefore for the same HBT size and tuning range, we can use a smaller size varactor. Since MOS varactor at millimeter-wave frequency is very lossy, the above design strategy leads to higher oscillation power at 80 GHz. In addition, the oscillator has two common-base cascode stages in parallel (Q_3~Q_6). Q_3 and Q_4 increase the generation of the 2^{nd}-harmonic signal at 160 GHz, which is further amplified by a casocode buffer. For the VCO at the bottom in Figure 5.6, Q_5 and

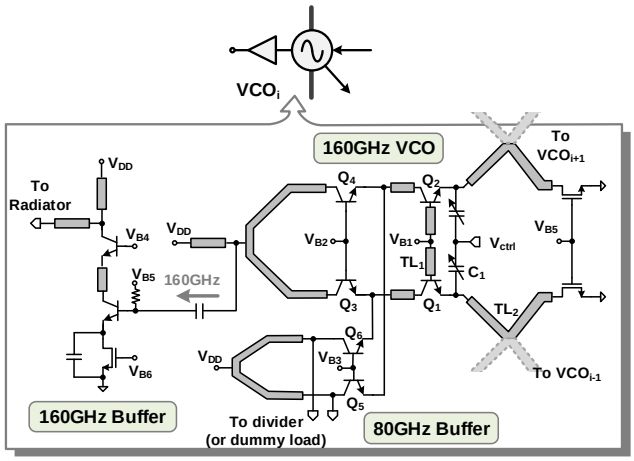


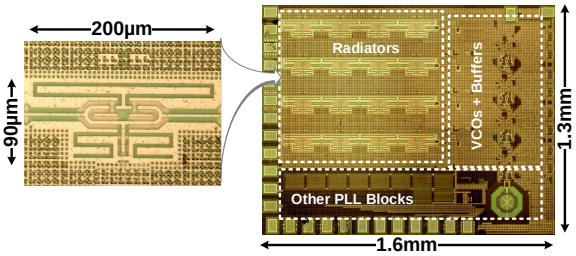
Figure 5.9: The schematic of the 160-GHz VCO inside the on-chip phase-locked loop.

Q_6 are used as a differential buffer to provide the 80-GHz output to the divider chain inside the PLL.

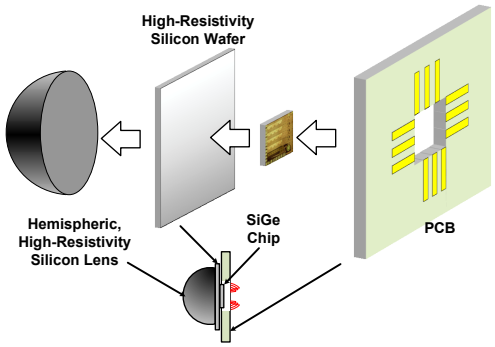
Between the adjacent VCOs, a tight coupling is obtained by directly connecting the intermediate nodes of their transmission line TL_2 at the emitters of the core HBTs (Figure 5.9). Similar to the radiator coupling described in Section 5.2.2, the VCOs are coupled with in-phase mode, and the coupling boundaries present open (hence has no impact other than phase alignment) to the VCO circuit. Since each VCO is coupled to its neighbors, and the only global signal routing is the low-frequency varactor bias control V_{ctrl}, this proposed PLL architecture is highly scalable, and can accommodate even bigger radiator size.

5.3 Prototype And Experimental Results

The proposed 320-GHz transmitter is implemented using a 130-nm SiGe:C BiCMOS process (f_T/f_{max}=220 GHz/280 GHz [125]). The microphotographs of the



(a)



(b)

Figure 5.10: (a) The microphotograph of the 320-GHz transmitter using 130-nm SiGe BiCMOS process. The THz radiator based on the return-path gap coupler is also shown. (b) The chip packaging with the backside attachment of a silicon lens.

chip as well as a THz radiator unit, are shown in Figure 5.10(a). The entire chip, including the 4×4 radiator array and the PLL, occupies an area of 1.6×1.3 mm^2. The chip packaging is shown in Figure 5.10(b). First, the chip is mounted onto a high-resistivity silicon wafer (~1 cm^2). The wafer is then glued to a PCB with a hole, so that the exposed front side of the chip is wire-bonded to the metal leads on the PCB for the connections of DC power supply, bias, and the PLL reference clock signal. Finally, a hemispheric, high-resistivity silicon lens (with a diameter of 1 cm) is fixed on the other side of the wafer after alignment. Compared to the radius of the lens (5 mm), the distance between the THz radiator and the spherical center of the lens is small (0.4 mm). Therefore, the beam collimation effect due to the lens is not significant.

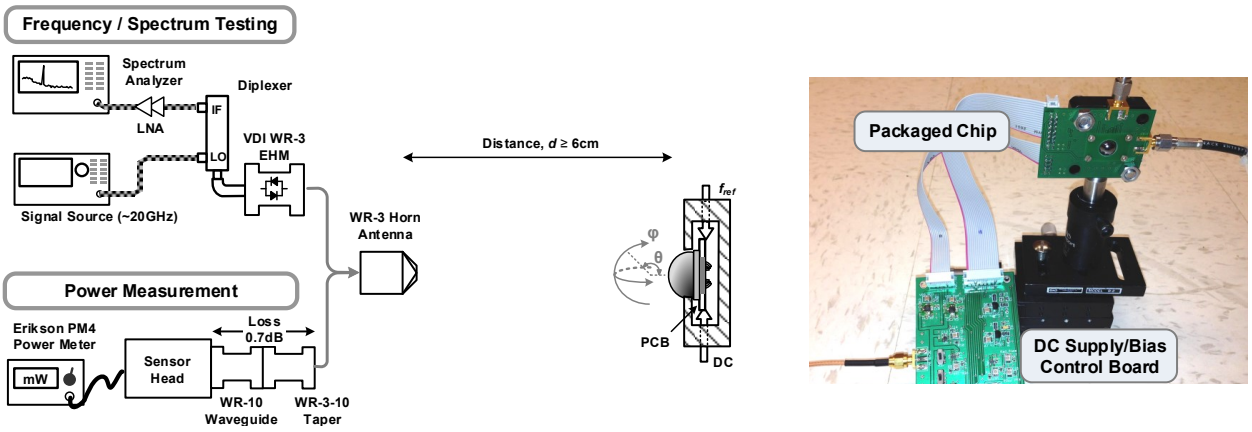


Figure 5.11: The measurement setup for the 320-GHz transmitter and a photo of the packaged chip.

The measurement setup is shown in Figure 5.11. The output THz beam of the chip is received by a diagonal horn antenna. For testing the frequency and spectrum of the radiation, a VDI WR-3.4 even-harmonic mixer (EHM) is used to mix the input THz signal with the 16^{th} harmonic of an externally-applied LO signal (~20 GHz). The measured spectrum of the down converted IF output is shown in Figure 5.12. When the on-chip PLL is turned off, radiator units are not synchronized and oscillate at their own free running oscillation frequencies. This is indicated in the multiple spurs in Figure 5.12(a). The number of spurs does not equal to the number of radiators (N=16); this may be due to the mutual pulling between some of the radiators through the silicon substrate. When the on-chip PLL is turned on, a single, coherent radiation is measured, as shown in the spectrum in Figure 5.12(b). Due to the constructive power combining, the output power is 7-dB higher than the radiation measured in the former case. The measured phase noise of the radiation is -79 dBc/Hz at 1-MHz offset.

Next, an Erikson power meter (with a WR-10 interface) is used to measure the absolute power level of the radiation. Shown in Figure 5.11, an additional

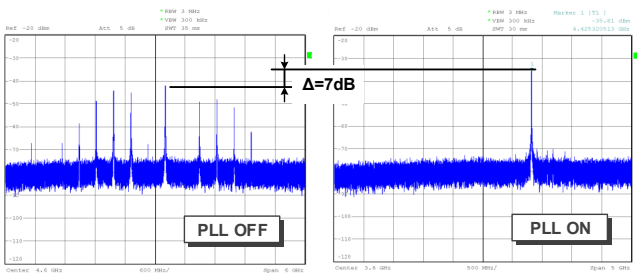


Figure 5.12: The measured down-converted spectrum of the transmitter radiation: (a) on-chip PLL is OFF and (b) on-chip PLL is ON.

1" WR-10 waveguide is used to protect the metal flange of the sensor head, and another 1" WR-10 to WR-3.4 taper is used to connect to the WR-3.4 horn antenna with a smooth transition. The total loss of such additional connection is 0.7 dB. To begin with, the distance between the 320-GHz transmitter and the horn antenna, d, is changed from 4 cm to 9 cm. The associated power received by the horn antenna, P_r, is plotted in Figure 5.13. It can be seen that when the distance is larger than 6 cm, the roll-off of the received power complies with the Friis transmission equation ($P_r \propto d^{-2}$ [137]). Because of this, all the subsequent measurements are based on the far-field distance limit of 6 cm. With this distance, the received power is 61 μW, resulting in a transmitter effective isotropic radiated power (EIRP) of 22.5 dBm.

Using the harmonic mixer, the radiation pattern of the transmitter is measured by rotating the chip in both azimuth φ and elevation θ directions (Figure 5.11). When the silicon lens is attached on the back side of the chip, the radiation pattern is shown in Figure 5.14(a). The measured directivity is 17.3 dBi and the 3-dB beamwidth is $\pm 10^{\circ}$. Such high directivity is due to the coherent 16-element array configuration, and is consistent with the simulation in Section 5.2. In addition, the radiation performance without the backside silicon lens is also characterized. It is expected that the output beam will undergo more

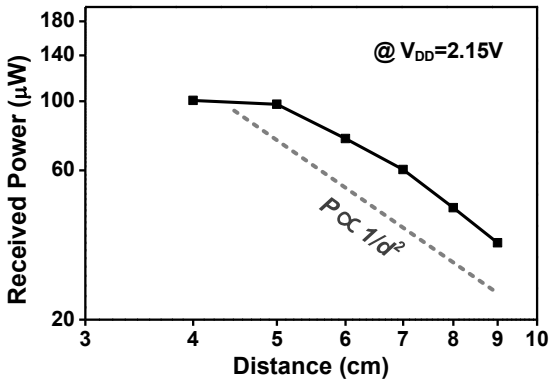


Figure 5.13: The received radiated power of the power meter at varying distance, d, from the 320-GHz transmitter chip.

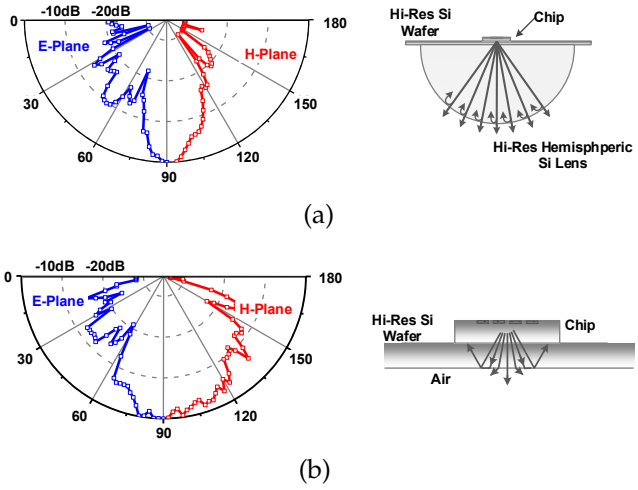


Figure 5.14: The performance of the state-of-the-art THz radiator sources in silicon (a) the total radiated power (b) DC to THz radiation efficiency.

divergence at the silicon-to-air interface, due to the more significant refraction near the critical angle (θ_c=16° [124]). Nevertheless, the measured pattern shown in Figure 5.14(b) still has a high directivity of 13 dBi, with an associated 3-dB beamwidth of ±27° (H-plane) and ±13° (E-plane). The asymmetric profile is due to the different reflection rates for s-polarized wave and p-polarized wave [127].

Finally, the supply voltage of the transmitter, V_{DD}, is swept. The associated

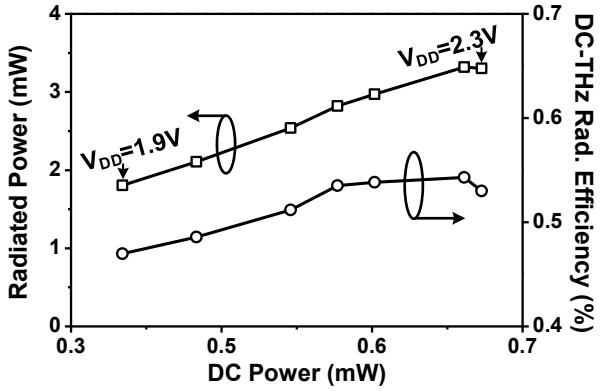


Figure 5.15: The total radiated power of the 320-GHz transmitter, as well as the associated DC-to-THz radiation efficiency, at different DC power supply voltage and dissipation power.

total radiated power, DC power consumption, as well as the DC to THz radiation efficiency, are plotted in Figure 5.15. Here, the total radiated power of the chip equals to the measured EIRP subtracted by the measured directivity. At the V_{DD} of 2.15 V, the total radiated power reaches its maximum of 5.2 dBm (3.3 mW), and the associated DC power is 610 mW. This leads to a DC to THz radiation efficiency of 0.54%. It is noteworthy that even when the backside silicon lens is removed, the measured total radiated power and the DC to THz radiation efficiency are still as high as 0.9 dBm (1.2 mW) and 0.2%, respectively. Such small degradation indicates that when a highly directive beam (perpendicular to the silicon-air interface) is generated from a large-array configuration, the undesired impact of the refraction and internal reflection (i.e. substrate-mode wave) is less significant. This should eventually lead to an efficient on-chip radiation without the need for a silicon lens.

5.4 Conclusions

This work achieves one of the highest radiated powers and DC to THz radiation efficiency numbers among all Si/SiGe technologies. Without the silicon lens, the output power is higher than most of the other radiators (only 0.1-dB lower than [126], which operates at a lower frequency and uses a faster SiGe process). Therefore, the proposed radiator design based on the return-path gap coupler has fully optimized the THz generation potential of the silicon transistors. It is also noteworthy that the proposed device analysis approach and radiator design can be applied to other integrated circuit technologies.

CHAPTER 6

LOW POWER NEGATIVE INDUCTANCE INTEGRATED CIRCUIT FOR GHZ APPLICATIONS

6.1 Introduction

In recent years, non-Foster circuits have attracted a great deal of attention due to their capability to overcome the gain-bandwidth limitation. It is well-known that all passive networks are bound by this limitation, and therefore any increase in the bandwidth results in a lower gain, and vice versa. However, with the use of non-Foster circuits, it is possible to simultaneously improve both gain and bandwidth. Non-Foster elements are capable of neutralizing the inductive or capacitive properties of any passive networks, such as matching networks, antennas, and impedance surfaces, over a wide range of frequencies by providing negative inductors or negative capacitors. These active negative elements can be synthesized using Negative Impedance Converters (NIC). In 1954, Linvill designed the first working transistor-based NIC circuit which was capable of providing negative resistance for low frequency operations (below 1MHz) [139]. The design was based on Open Circuit Stable (OCS) operation, implying that the circuit is stable only when there is relatively large impedance across the port. Recently, Sussman-Fort and his colleague have shown that the bandwidth characteristic of an electrically small antenna can be significantly enhanced using non-Foster circuits [140]. In their paper, a non-Foster circuit which is capable of providing a negative capacitor in the frequency range of 20 MHz to 100 MHz is designed and implemented using discrete components. However, with the advancement in silicon technology, more practical integrated non-Foster cir-

cuits can be designed and implemented for a wide range of applications. For instance, at high-frequency applications (above 1GHz) where the impedance of the load is not purely resistive, a non-Foster matching circuit can be used to maximize the power transfer between the source and the load. Non-Foster circuits can also be used to achieve electrically small broadband antennas, as well as wideband metamaterials and metasurfaces [141],[142].

6.2 Negative Impedance Converter Design

Up to this date, researchers have theoretically analyzed many different implementations of NIC circuits. However, only few have built and tested their circuits to verify that they can provide a low loss and stable output at high frequencies [140], [143], [144]. In this paper, an NIC circuit based on Linvill's open circuit stable topology is proposed. The design is fully CMOS compatible, which allows having a device with lower power consumption compared to its BJT and BiCMOS counterparts [145]. The core of the NIC is a cross-coupled differential pair of n-MOS transistors as shown in Figure 6.1(a). The NIC converts the load impedance seen by the drain of M1 and M2 to its negative equivalent at the input terminal. To investigate this analytically, a small signal model is developed as shown in Figure6.1(b), and the input impedance of the NIC (Z_{in}) is obtained in terms of the load impedance (Z_L) [141].

$$Z_{in} = \frac{2r_0}{1 + g_m r_0} + \frac{z_L}{1 + g_m r_0} - \frac{Z_L g_m r_0}{1 + g_m r_0} \tag{6.1}$$

where r_0 and g_m are the transistor's output resistance and transconductance, respectively. Assuming $g_m r_0 \gg 1$, equation (1) can be approximated as

$$Z_{in} = \frac{2}{g_m} - z_L \overset{g_m \gg 2}{\Longrightarrow} Z_{in} \simeq -Z_L \tag{6.2}$$

From (2) it can be seen that the obtained negative impedance comes with a resistance of $\frac{2}{g_m}$ which can be minimized by increasing g_m.

6.3 Negative Inductor Implementation

A practical implementation requires a number of design considerations, such as biasing circuits, transistor's type, and transistor's aspect ratio to name a few. All these parameters should be chosen carefully in order to achieve a linear, stable output with minimal noise.

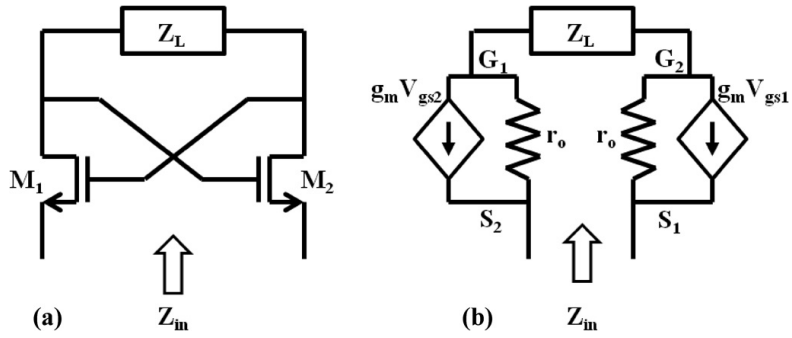


Figure 6.1: A Basic non-Foster element, (a) Negative Impedance Converter circuit implementation based on Linvill's OCS model, (b) the equivalent small-signal model of the proposed NIC based on CMOS technology.

6.3.1 Biasing Circuits

First, a self-biased current source, which is typically less sensitive to the supply voltage fluctuation, is chosen for this task [146]. Figure 6.2 illustrates the schematic of a self-biased current source. In addition, analysis shows that the

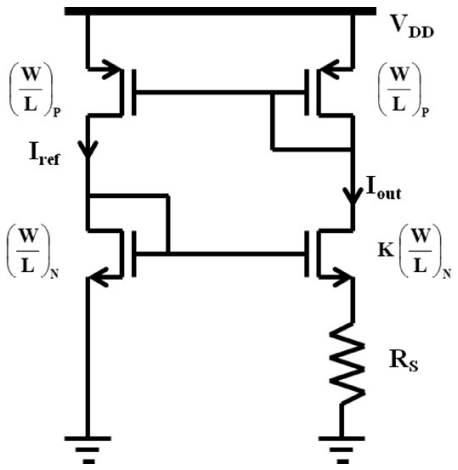


Figure 6.2: Schematic for the self-biased current source using an on-chip resistor Rs.

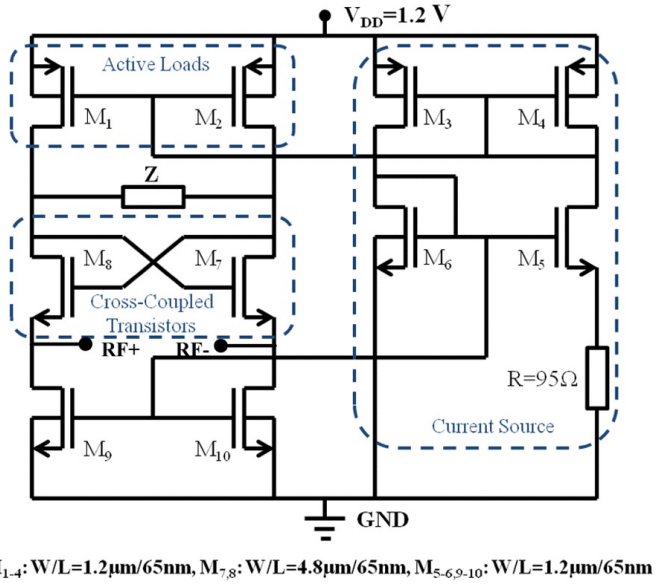


Figure 6.3: Schematic diagram of the Negative Impedance Converter (NIC) integrated circuit which has been implemented in a 65 nm process and it produces a negative inductance of $L = -1nH$.

output current, I_{out}, can be obtained as follows:

$$I_{out} = \frac{2}{\mu_n c_{ox}(\frac{w}{l})R_s^2}(1 - \frac{1}{\sqrt{k}})^2 \tag{6.3}$$

where μ_n, c_{ox} and $\frac{w}{l}$ are the electron mobility, oxide capacitance and transis-

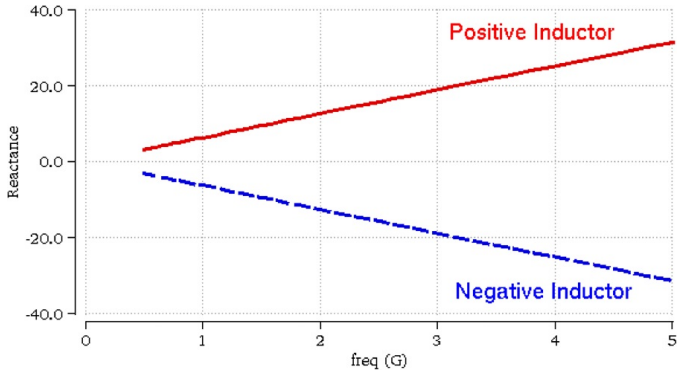


Figure 6.4: Reactance vs. frequency for both positive inductor (solid red curve), and negative inductor (dotted blue curve).

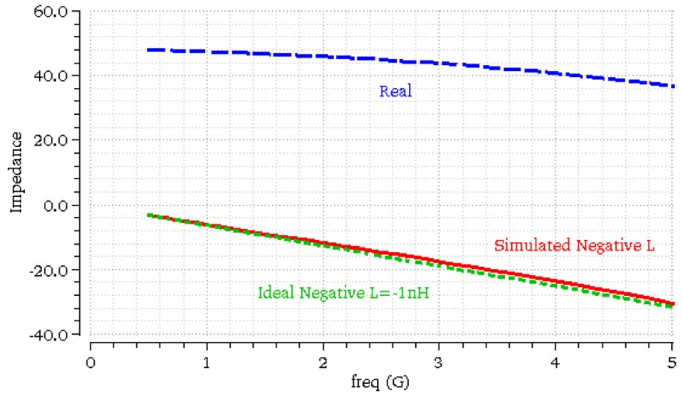


Figure 6.5: Negative inductance simulation ($L = -1nH$) with a real part of approximately 45 Ω (dashed blue), imaginary part equal to $L = -1nH$ (solid red), and ideal imaginary part for $L = -1nH$ (dotted green).

tor's aspect ratio, respectively. Then, high impedance active loads are placed between the cross-coupled transistors and the power supply in order to avoid having a short circuit RF signal. Note that these active loads must present very high impedances in order to reduce loading effects at the NIC output. Current mirrors are then attached to the bottom of the cross-coupled transistors to provide the current through which g_m of cross-coupled transistors is determined. The complete schematic of the proposed NIC circuit is illustrated in Figure6.3, which includes a self-biased current source, active loads, a current mirror and a

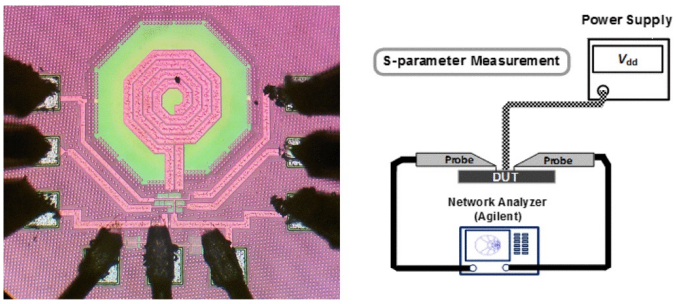


Figure 6.6: Microphotograph of the proposed negative inductor design including GND, Power and RF pads (left), and measurement setup (right).

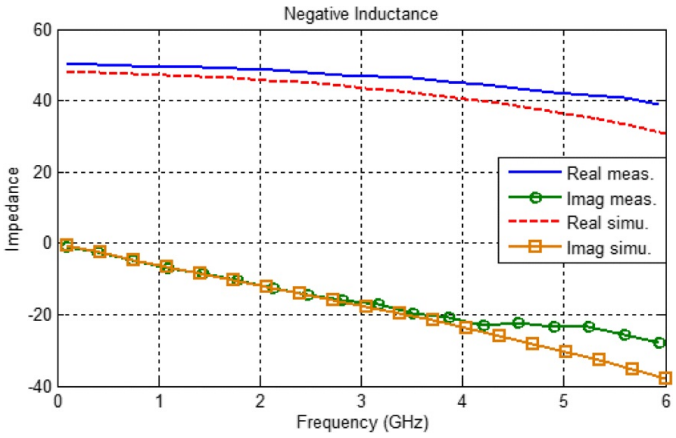


Figure 6.7: Comparison of the measured and simulated (Spectre-RF) impedance of the negative inductance circuit ($L = -1nH$).

general load of Z. In this design, the self-biased current source provides a current of 1.7mA resulting in a transconductance of g_m=30mS for the cross-coupled transistors.

6.3.2 circuit simulation

In this section, the implementation of a negative inductor is demonstrated in detail. A negative inductor has the same magnitude of reactance compared to

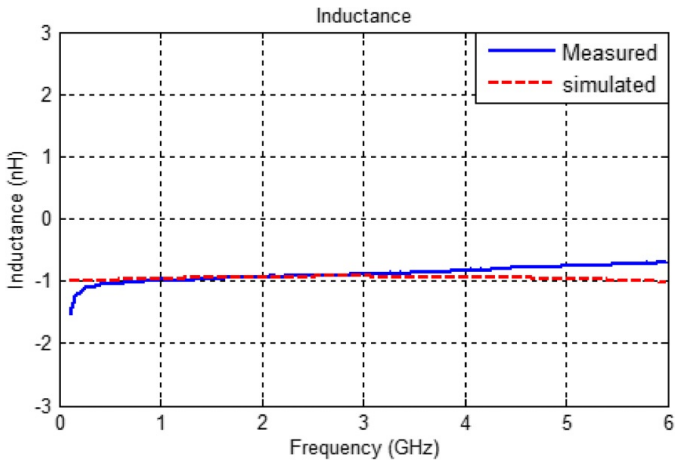


Figure 6.8: Measured and simulated results for the negative inductance.

a positive inductor, but with the opposite sign. Figure 6.4 demonstrates the behavior of the positive and negative reactance for an inductor. The configuration shown in Figure 6.3 is used to obtain the negative inductor by replacing the general load (Z) with an inductive load of $L = 1nH$. As expected, the NIC will produce a negative load equivalent to $L = -1nH$ at its output, as marked by RF+ and RF-. Figure 6.5 illustrates the simulated negative inductance obtained by Spectre-RF [147]. The simulation also shows that the NIC consumes 5.1 mW of power when it is connected to a 1.2 V power supply, and that the output noise voltage is 0.75, 0.70, and 0.65 $nV/\sqrt{Hz}$ at 0.1, 1, and 3 GHz, respectively at 27C.

6.4 Fabrication and Measurement Result

The negative inductance design shown in Figure 6.3 has been fabricated in a 65nm CMOS process on a 0.3×0.3 mm^2 die. Figure 6.6 demonstrates the microphotograph of the fabricated negative inductance design, along with its measurement setup.

The prototype was measured using an Agilent E8364B Vector Network Analyzer (VNA), and a 1.2 V DC supply was used to power up the chip. The differential nature of the NIC output port requires the use of two Ground-Signal-Ground (GSG) probes. These probes are attached to the VNA ports with an impedance of 50Ω. Probe tips are then calibrated prior to the measurement by performing the short-open-load calibration. Figure 6.7 compares the measured and simulated (Spectre-RF) impedance of the negative inductance circuit operating from 0.1 GHz to 6 GHz. Furthermore, the equivalent inductance is extracted as a function of frequency, and a relatively constant negative inductance is observed over the same range of frequency as shown in Figure 6.8.

6.5 Discussion

The simulated and measured results are in excellent agreement for a wide range of frequencies from 100 MHz - 6 GHz. At higher frequencies, a slight variation is observed which is primarily due to parasitic effects and possibly the test set up. The Open Circuit Stable (OCS) condition implies that the NIC is stable when the load connected to the NIC is large compared with the NIC impedance. In other words, the NIC output impedance should be relatively small compared to the load in order for the design to remain stable. The resistance associated with the negative L, which is inversely proportional to the transconductance of the cross-coupled transistors as formulated in (2), varies from 40 Ω to 50 Ω for the proposed design. In order to reduce this resistance, one can increase the g_m by injecting more current into the cross-coupled transistors at the cost of increasing power consumption. Therefore, there is a trade-off between power consumption, chip size, and loss.

CHAPTER 7

CONCLUSION AND FUTURE DIRECTIONS

In this thesis we have introduced new approaches to design high speed electronic circuits. We show how by accurate characterization of electronic devices, the performance of high speed circuits can be improved. In the proposed approaches we blend multiple disciplines, e.g., analog circuit design, device physics, electromagnetic and applied mathematics.

For design of high frequency and high power electronic circuits, we propose a systematic design approach which employs a new nonlinear device model. The proposed nonlinear power modeling facilitates the design of blocks and systems where the harmonic content of the signal is important. Harmonic enhancement techniques can be performed more precisely in different classes of power amplifiers to improve the efficiency. Harmonic suppression in fundamental oscillators based on Manley-Row principle enhances the fundamental power efficiency. In other words, a harmonic power suppression based on a nonlinear model leads to design of more efficient local oscillator circuits. As a summary, by capturing the harmonics behavior in nonlinear circuit blocks, the performance of transceivers, communication links and imaging circuits at mm-wave and sub-mm-wave range is enhanced.

The proposed nonlinear design approach can be applied to emerging technologies. III-V compound semiconductor devices, e.g., GaN and InP, exhibit a larger bandgap compared to the existing Silicon technologies. The intrinsic superior electron mobility in N-type devices provides a high cut-off frequency

(f_{max}) and makes them a good candidate for Terahertz applications. Additionally, equipped with a higher break-down voltage, these devices are well-suited as the future platform of high power Terahertz implementation. Therefore, devices such as High-Electron-Mobility transistors (HEMT's) have been developed to pave the path towards high frequency applications. GaN transistors with a Johnson's Figure of merit of 27.5 times larger than Silicon, enhance the power levels and operation frequencies of high speed electronic circuits significantly. Despite the mentioned advantages of the compound devices, their operation beyond f_{max} requires a nonlinear model to capture the harmonic dynamics. Taking advantage of my proposed technique to characterize the nonlinear profile of transistor, future Terahertz electronic circuits can reach beyond 1 THz of operation frequency and the unwanted gap of optics and electronics, Terahertz Gap, will further shrink.

Terahertz waves exhibit a superior resolution compared to lower frequency components and leave the material non-ionized in contrast to X-ray imagers. Due to the plethora of water absorption bands from 300 GHz to 3 THz, sub-mm-wave imaging is suitable for biomedical applications. In particular "cancer tumor monitoring", "in-vivo tooth cavity detection" and "spectroscopy" can be implemented, should there be sufficient generated power at this frequency range. The proposed nonlinear Terahertz design techniques, pave the path towards the implementation of high power integrated circuits with sufficient output power. It is noteworthy that the antenna elements at this frequency range can be eaisly fit on the silicon chip and a fully integrated design is possible. Last but not least, these integrated circuits can be packaged to be utilized in-vivo for sensitive monitoring applications and simplify the tracking of different biomed-

ical mechanisms and organs.

In the domain of high speed computation, we have proposed another benchmark application of spin devices which exploited their intrinsic features. We selected "non-Boolean computation" since the non-volatile profile of all-spin devices simplifies the implementation of majority gates and comparators. Called "Smart Detector Cell", the system performs pattern recognition on matrices of binary images within a few nanoseconds and returns the number of mismatches in a non-Boolean scheme. This circuit outperforms CMOS counterparts in terms of DC power consumption, computational complexity, processing time and effective area. To the best of our knowledge, this system is the first all-spin circuit to perform binary image recognition.

By introduction of "approximate computers", certain problems such as monitoring and tracking can be performed 100 times faster than conventional processors. Search engines may not also find the exact match of an input query; however, they can find many acceptable answers using non-exact techniques. All-spin circuits such as adders, multipliers and non-volatile storage units are the key building blocks of an approximate computer, which is in principle capable of implelmenting most machine learning algorithms. Operating at lower voltages, these units are ultra-low power and exhibit a high integration density. Our proposed all-spin pattern recognition circuit also performs a non-Boolean approximate computation and can be utilized in the design of future artificial intelligence units such as neural networks. In addition, the non-volatility of spin devices, facilitates the implementation of exact and approximate storage units which are the key to training complex models such as deep neural networks. Ultimately, these systems are expected to mimic the operation of human

brain for pattern recognition applications and pave the path towards the more efficient implementation of “Human-Machine Interface”.

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